Study on Variable Rotation Polishing Method in Chemical Mechanical Polishing

著者	Pipat Phaisalpanumas
year	2015
その他のタイトル	CMPにおける可変回転ポリシング法に関する研究
学位授与年度	平成26年度
学位授与番号	17104甲情工第301号
URL	http://hdl.handle.net/10228/5459

Study on Variable Rotation Polishing Method in Chemical Mechanical Polishing

by

Phaisalpanumas Pipat

Submitted to the Department of Information Systems
in Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY IN INFORMATION SYSTEMS

Graduate School of Computer Science and Systems Engineering

Kyushu Institute of Technology

2015

Abstract

Study on Variable Rotation Polishing Method in Chemical Mechanical Polishing

by

Phaisalpanumas Pipat

Variable rotation polishing (VRP) method is proposed in order to improve polishing performance such as material removal rate (MRR). The VRP method is characterized as a combination of the additional backward rotation with the forward rotation only (i.e. the conventional polishing). The MRR increases as the angle of additional backward rotation becomes higher until 360 degrees. In that case, the MRR of the VRP method was 38 percent higher than that of the conventional polishing.

Asperity of polishing pad surface is one of the dominant parameters affecting the MRRs and stabilities of the Chemical Mechanical Polishing (CMP) process. According to the investigation of a polishing pad surface topography suggests that the asperity of the polishing pad surface was kept standing upright by backward rotation of the polishing pad. Particularly, the peak area of the asperities on polishing pad surface, the roughness became higher in the VRP method than in the conventional method. This result predicts that there are more the number and the area of the polishing pad asperities, which would approach near to the wafer surface being polished, are kept standing upright in the VRP method. Therefore, these asperities was able to consequently sustain the MRRs. In other words, this behavior suggests that in the VRP method, the preservation of the asperity on polishing pad surface would sustain the MRR because of the backward

rotation, which may contribute to the realization of a polishing pad conditioning treatment-free CMP process. This feature also indicates that this method could result in the longer polishing pad life, namely the cost reduction of polishing pad.

Slurry flow distribution and slurry film thickness were also evaluated in the VRP method comparing to the conventional polishing method. The slurry flow distribution was analyzed through a transparent quartz substrate by a high-speed camera. The slurry flow distribution of the VRP method was not uniform as compared with the conventional method, although the MRR of the VRP method was higher than that of the conventional method. The slurry film thickness variation was measured using a surface scanning laser confocal displacement meter on the upper surface position of a quartz substrate with and without slurry. The position of a quartz substrate varied from 9 μm to 8 μm during the CMP process. This implies that the slurry film thickness in the VRP method was 1 μm thinner than that of the conventional polishing. These results suggest that these 2 parameters are not dominantly effective against the MRR of the CMP process.

As above mentioned, the preservation of the asperity on polishing pad surface is one of the dominant parameters to sustain the MRR.

Keywords: Variable Rotation Polishing, Chemical Mechanical Polishing, CMP process, Material removal rate, Polishing pad, Slurry, Asperity

Acknowledgements

I would like to begin by thanking my advisor Associate Professor Dr. Keisuke Suzuki for his divine guidance and friendship over the 4 years I have known him. He truly provided me with an experience that very few live through and I will never forget him for that. Thank you for preparing me for the long road ahead. I would also like to extend many thanks to Professor Dr. Takahiro Ito, Professor Dr. Eiji Hayashi, Professor Dr.Takashi Okamoto, Professor Dr. Keiichi Kimura and Assistance Professor Dr. Panart Khajornrungruang for your inspiration, motivation, teaching, terrific guidance over the course of my graduate work. I would like to also thank my past and present colleagues Mr. Takashi Kushida, Mr. Shintarou Isono, Mr. Takahiro Tajiri and Mr. Yuuichi Takano. In particular I would like to thank Mr. Kazuki Soejima, Miss Sukanya Noichan, Mr. Amornphun Phunopas, Miss Chulaluck Laohawattanapinyo, Mr. Aphaiwong Junchangpood, Miss Shunen Kyo, Mr. Wisanu Jitviriya, Mr. Sakmonhkon Chumkamon, Mr. Sirichai Tammaruckwattana and Miss Vilasinee Leowarin they have been a great friends, colleague and I wish them the best of luck in their journeys ahead.

To the faculty and staff. I have been in the Department of Information Systems, Faculty of Computer Science and Systems Engineering, Kyushu Institute of Technology for four years. Everyone who has come and gone has been a significant help to me. I have had the incomparable chance to interact and know each of you not only as students, but as friends.

To all my friends I thank you all for keeping me sane amidst all the stresses and pressures in life. I would also like to thank Thai friends,

although I have no idea what future lies ahead for you, I wish you the happiest of lives. You were the biggest influence in my life.

Finally, I would like to give my greatest thanks to my family. They have all collectively inspired and encouraged me to get where I am today and there is nothing in the world that I could do or give that would make up for all the time and energy you have put into me. Thanks for always picking me up when I was down and always making me feel loved and happy. I wish you all the healthiest, happiest and most fruitful years ahead.

Phaisalpanumas Pipat

March 2015

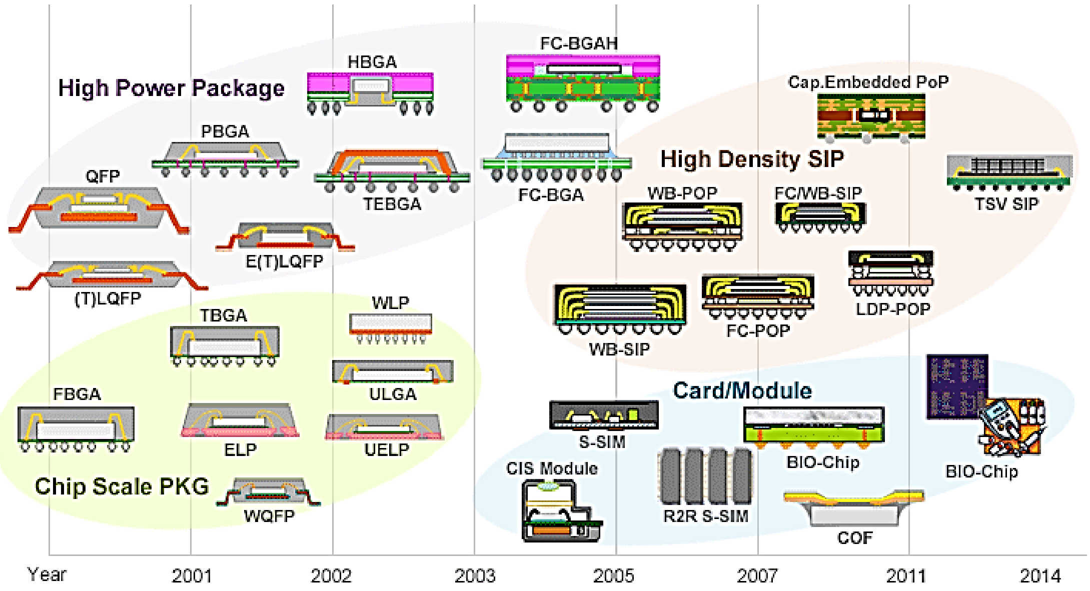
Table of Contents

Chapter 1

Introduction

1.1 Background

In the last two decades, the development of semiconductor devices such as smart phones has been remarkable where the processing speed and memory size is increased by a year, owning to Ultra Large Scale Integration (ULSI) which was realized by the shrinkage of transistor gate size, hence billions of transistors on the IC chip. Moreover, the scale of transistor gate size reduces the device size in overall, thereby increasing the packing density and enhancing the cost performance. Additionally, the processing speed of an electronic device, which is inversely proportional to the gate size, has been enhanced, as well as the power consumption which is approximately proportional to the square of gate size has gain improvement. Along with the development of semiconductor devices, the complexity of microchip design and fabrication have increased continuously as the integration and miniaturization of microchips developed, as shown in Figure 1.1. Extremely high degrees of repeatability and uniformity are required in wafer fabrication for a high production throughput.



From: http://www.samsung.com/global/business/semiconductor/foundry/service/back-end-service.

Figure 1.1: History of semiconductor device [1]

The increase of process speed of an IC chip lies in the multi layered structure and interconnections. The time delay constant of an IC chip is represented by the product of the resistance and capacitance thereof, or by RC delay τ, as expressed in Equation 1.1 [2]:

$$\tau = RC = \rho k \frac{l}{d} \qquad \text{Equation 1.1}$$

where ρ is resistivity, k dielectric constant, l resistance length, and d capacitor distance. In order for RC delay to be small, the material for interconnects and interlayer dielectric needs to have as low resistivity and dielectric constant as possible, while the length of gate size and the distance of dielectric stand in a tradeoff relationship. As the interlayer dielectric or low-k material, silicon oxide film is generally used. Although aluminum was used as the interconnect material in the earlier period, copper has nowadays replaced aluminum due to its lower resistivity than the former. Furthermore, although the interconnecting process is used to be carried out by applying Reactive Ion Etching (RIE) on an aluminum layer deposited through Physical Vapor Deposition (PVD), the Cu dual Damascene process, where copper interconnects are embedded in dielectric trenches since copper can hardly be dry-etched, as shown in Figure 1.2. The multilayered structure of an IC chip is realized nowadays by the Chemical Mechanical Planarization technology which is a selective polishing method realizing global/local planarization on the wafer.

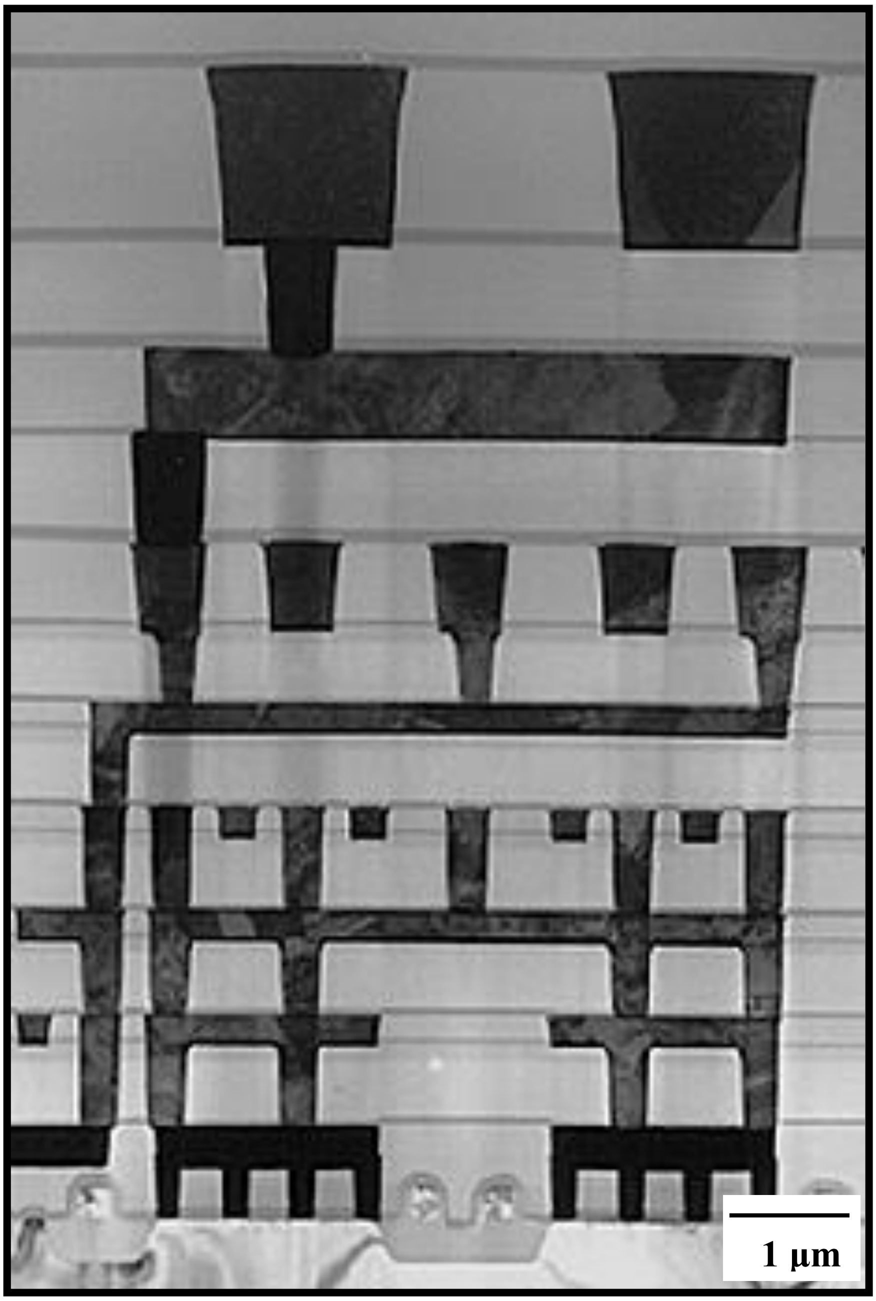
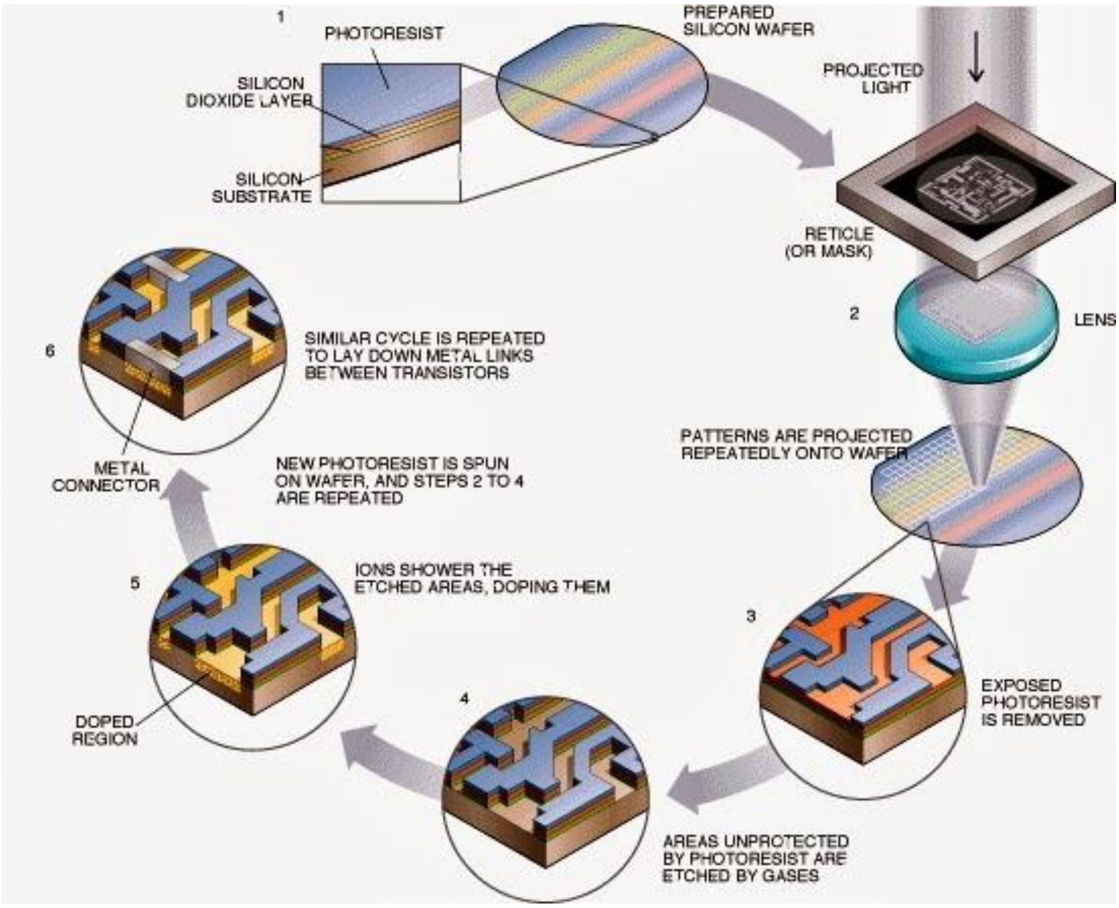


Figure 1.2: Cross-section TEM photograph of Cu multilayer interconnect [3]

1.2 The Role of CMP in Semiconductor Manufacturing

There are two major applications of CMP in ULSI manufacturing: to smooth surface topography of inter-level dielectrics (ILD, usually silicon dioxide) or to remove excess material to produce inlaid metal structure or isolation trenches. The inter-level dielectric CMP is applied in conventional aluminum metallization where the aluminum is deposited on the oxide ILD layer, patterned, and etched to form interconnects. Another layer of oxide is then deposited to insulate the aluminum interconnects. Thus three-dimensional electrical wiring is constructed. Device elements such as resistors, capacitors and transistors are connected to build up ICs. In this practice, CMP is employed on at least the top few layers of each ILD surface to provide a smooth surface for aluminum deposition and to provide a field flat enough that contact vias and metal wires can be patterned by lithography. The desired process end-point is determined based on the surface planarity and the thickness of the ILD layer required for electrical isolation of aluminum line. Wafers stacked with three or more layers of aluminum interconnect, such as those used in microprocessor applications are usually subjected to ILD CMP to improve yield and reliability.

Unlike ILD CMP, copper CMP and other trench isolation processes such as shallow trench isolation (STI) are employed to remove the excess deposit covered on the trenches. The underlying oxide (or other ILD material) layer is trenched by lithography and etching. A thin copper layer is deposited or electroplated to fill the trenches. Then a CMP process removes excess copper and forms isolated wirings of copper. The process is stopped while the copper layer and diffusion barrier layer (usually a thin Ta, TaN, Ti or TiN layer to prevent copper diffusion into the oxide and "poisoning" the underlying devices) are completely polished through and the oxide is exposed. Copper technology is expected to replace aluminum in new-generation chips with interconnect critical dimensions (CDs) below 0.25μm. Since copper is difficult to pattern and etch the damascene approach and extensive use of the CMP seems to be the best solution for ULSI manufacturing. Figure 1.3 shows the main steps and sequence of the semiconductor manufacturing including Layering, Photo-lithography, Etching, Doping, Resist removal and Wafer cleaning. Layering techniques are used to grow thin layers of film on the surface of a silicon wafer. Photo-lithography is the process used in micro fabrication to selectively remove parts of a thin film. It uses light to transfer geometric pattern from a photo mask to a light-sensitive chemical (photo-resist) on the substrate. Etching is the process of using strong acid or mordant to cut the unprotected parts of a metal surface to create a design in intaglio in the metal. Doping refers to the process of introducing impurity atoms into a semiconductor region in a controllable manner in order to define the electrical properties of this region. After the etching or ion implantation step, the photoresist needs to be stripped away. Cleaning techniques are used to remove particulates and chemical impurities so contaminant-free surfaces can be obtained [4]. The details of the CMP process are described in Chapter 2.



From: http://rohitrana33.blogspot.jp/2013/10/introduction-of-semiconductor.html

Figure 1.3: The main steps of the semiconductor manufacturing

1.3 Origins and Evolution of the CMP Process

The conventional methods such as patterning directly on the thin film formed by CVD or PVD was no longer possible to correspond. Therefore, techniques are required to planarize the surface after forming a thin film by CVD or PVD, CMP techniques have been developed as shown in Table 1.1 [5].

CMP technique for purposes of the vertical planarization of the semiconductor integrated circuit is obtained by incorporating in the middle of the production process. Since at the time of polishing may dust occurs, sealed and by washing before unloading the wafer. It has become possible to bring the polishing machine in the clean room.

At the beginning, CMP has been incorporated into the manufacturing process. LSI is manufactured from aluminum and silicon oxide film. It has been limited to the application to a portion, such as tip LSI device that is effective to improve the yield in manufacturing. However, causing a problem of wiring between the delay due to the higher clocked, the copper damascene process is utilized, and the CMP process has become the essential process.

Table 1.1: Transition of the wiring width and miniaturization technology

<table>
<tr><th>Generation</th><th>~400nm</th><th>250nm</th><th>180nm</th><th>130nm</th><th>90nm</th><th>65nm</th></tr>
<tr><td>Lithography</td><td>i-line (365nm)</td><td colspan="3">KrF Excimer laser (248nm)</td><td colspan="2">ArF Excimer laser (193nm)</td></tr>
<tr><td>Planarization</td><td>BPSG reflow</td><td colspan="5">CMP</td></tr>
<tr><td>Insulating layer</td><td colspan="2">CVD</td><td colspan="4">HDP</td></tr>
<tr><td>Contact metal</td><td>PVD</td><td colspan="4">CVD</td><td>ALD</td></tr>
</table>

1.4 CMP process in the near future

Chemical mechanical polishing (CMP) is widely adopted in producing excellent local and global planarization of wafer surface for microelectronic devices and semiconductor manufacturing industry. The CMP process is required to planarize the overburden area in the interconnect process. It is a balanced polishing process that relying on chemical reaction of the slurry with the substrate, oxide, thin film and mechanical pressure on the substrate to a polishing pad to remove the passivation layer. However, the fundamental mechanisms of material removal and the interactions of the chemical and mechanical effects are not well understood [6-9].

Recently, the size of wafer used in semiconductor manufacturing industry has been changed from 300 mm to 450 mm, which would involve a significant investment tool and fabrication facilities. Therefore, some issues arise regarding whether the tools that are currently used for 300mm wafers could, in some cases, simply be scaled up or whether there are any problems occurred by doing so. For example, the slurry costs would become prohibitive due to the increase in the polishing pad area. Also, in the case of the conventional CMP tool the slurry may be unable to fill in the narrow gap between wafer and polishing pad around the center area when wafer size becomes larger [10, 11]. Initially, there was an attempt on the slurry supply issue around the center area as mentioned above by proposing the Variable Rotation Polishing (VRP) method in the CMP process.

Chapter 2

The Chemical Mechanical Polishing Technology

2.1 Chemical Mechanical Polishing

The requirements of wafer surface planarization in the semiconductor process include the realization of a flat and smooth surface with no contamination or defects such as scratches and deformities. Furthermore, in order to enhance cost performance and throughputs, wafer surface planarization must be achieved on larger wafers.

A basic configuration of Chemical Mechanical Polishing is shown in Figure 2.1. A CMP polisher consists of the platen, polishing pad, carrier, and conditioner. The wafer is held by the carrier which applies down pressure on the wafer. During polishing, the carrier rotates on the polishing pad, fixed on the platen which also rotates as the slurry is provided at the center of the platen. The conditioner is applied to the polishing pad before polishing in order to roughen the surface of polishing pad.

Generally, the size of wafers in the semiconductor industry is increased from 200 mm to 300 mm, and the wafer with diameter of 450 mm is nowadays introduced [10]. Naturally, the large wafers raise issues concerning polishing methods and conditions in order to maintain the high precision achieved by CMP. Note that as the size of wafer increases, the behavior of the slurry underneath and around the wafer and the thermal distribution of the slurry becomes different (i.e. it becomes hard for the slurry to flow underneath the entire wafer, and the temperature of the slurry is to some extent related to the chemical reaction which occurs on the wafer surface) as shown in Figure 2.2.

The polishing speed or Material Removal Rate (described as MRR in what follows) is empirically estimated by Preston's equation, as shown in Equation 2.1, which is proportional to the pressure and relative velocity by which the wafer is influenced [12].

$$\mathrm{MRR} = k \cdot P \cdot V \qquad \text{Equation 2.1}$$

where k is Preston coefficient, P is pressure, and V is relative velocity.

In addition, Figure 2.1 contains a close up view of the wafer surface to be polished. The chemical reaction layer is produced by the slurry particles in proximity to the wafer surface. In turn, the chemical reaction layer is removed by the movement of the slurry particles induced by the mechanical motion of the polisher. However, the mechanism of CMP is yet to be explained by a conclusive theory.

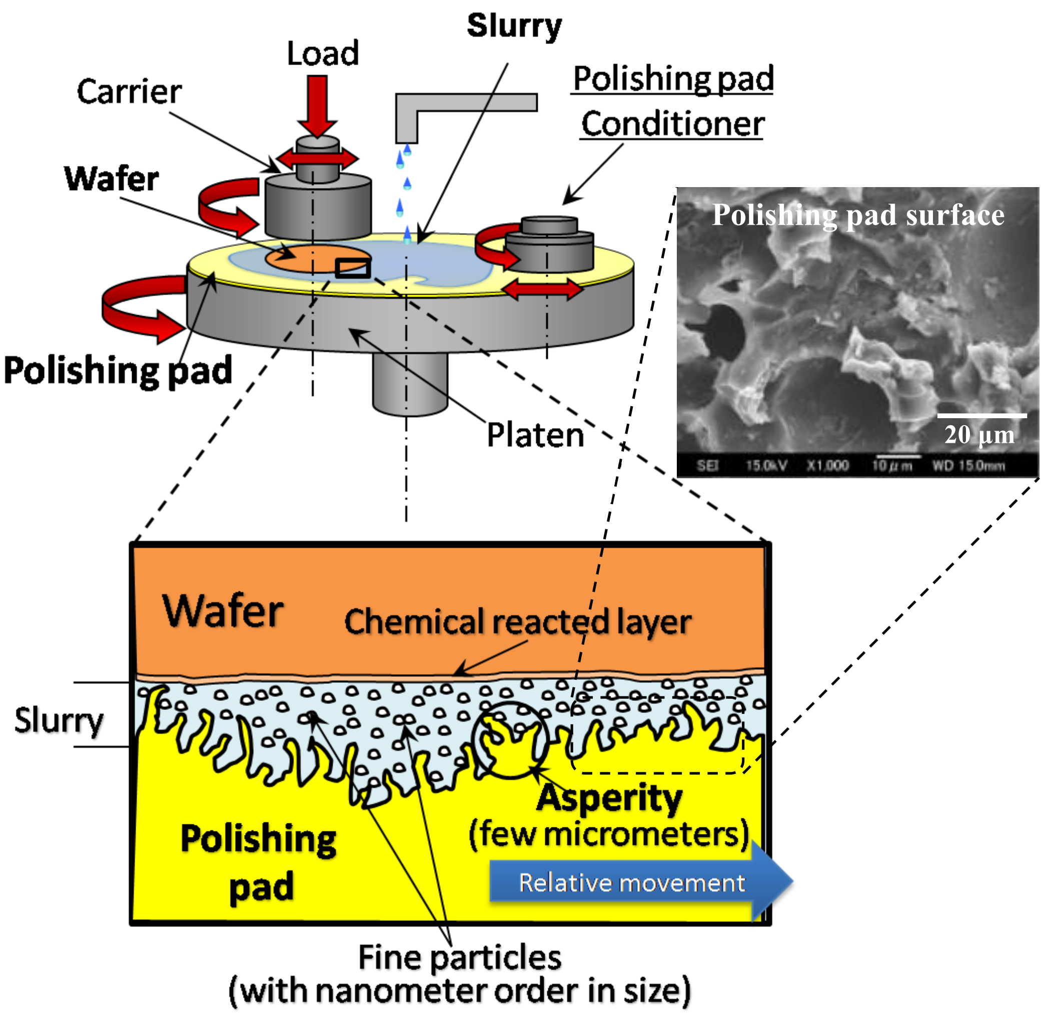


Figure 2.1: CMP configuration and close up view of polishing area

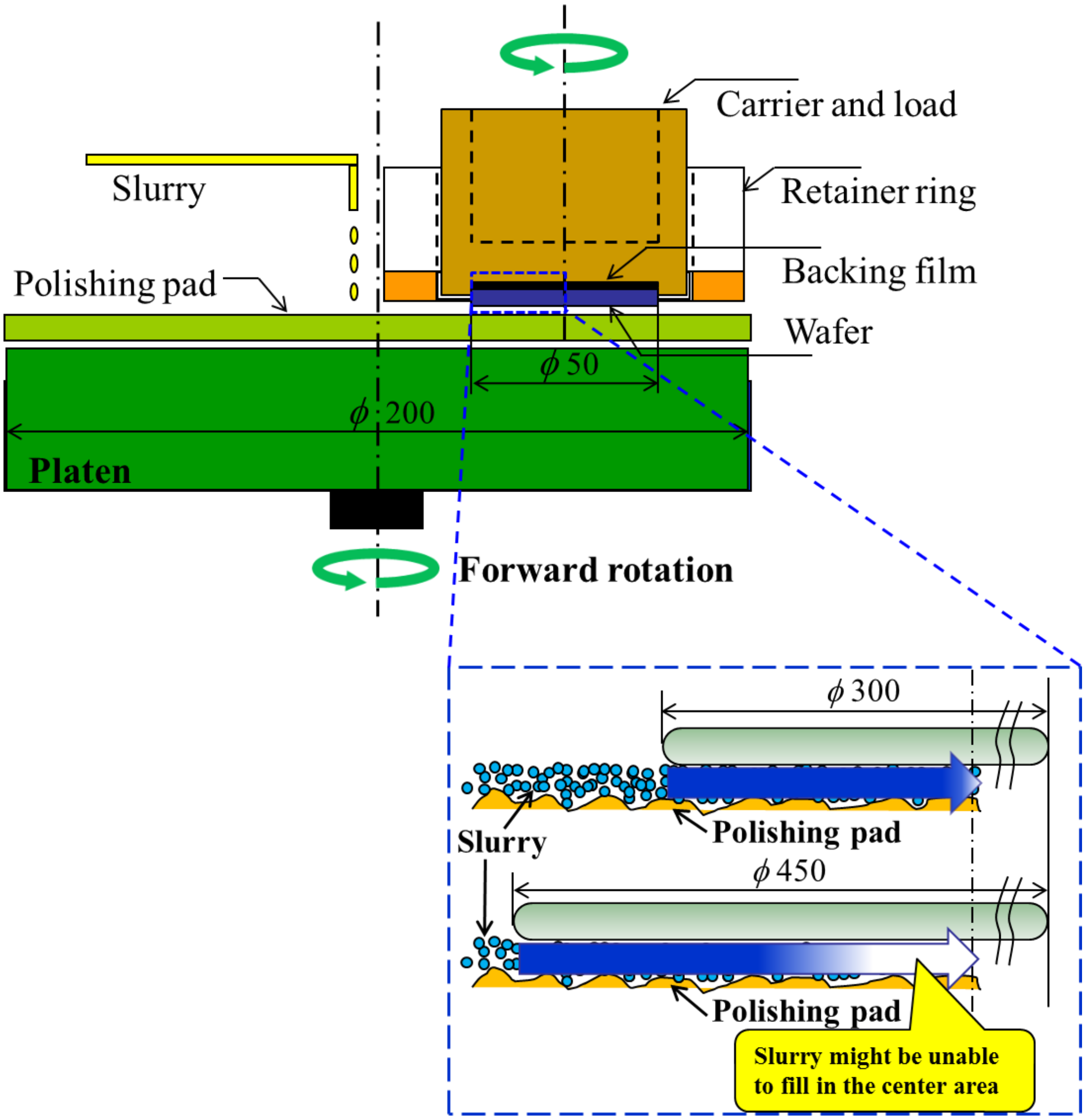


Figure 2.2: Chemical Mechanical Planarization configuration and slurry flow issue from the increased wafer size

2.2 Requirements of CMP

An ideal planarization of the wafer in the semiconductor manufacturing process is to achieve a planar surface across the entire wafer, on which all the protruding areas are primarily removed. It is a selective process, in contrast to the wet chemical etching which is isotropic. The selectivity of CMP is dependent upon the mechanical interactions of CMP, one of whose composites is the polishing pad. Generally speaking, in CMP, the wafer surface is polished by the relative movement caused by minute particles suspended in the slurry and the movement of the elastic polishing pad which is applied in the polishing process. The polishing pad wears during a CMP process due to the slippery friction between the pad and particles, which takes place when the polishing pad moves on the wafer. As polishing is carried out, due to wafer edge exclusion which is caused by a non-uniform distribution of the load across the wafer, several millimeters of the radial area of wafer is lost. Therefore, in order to achieve high flatness, the polishing pad needs to satisfy the criteria as follows:

1. The polishing pad needs to be thin, hard, and resist deformation.
2. Polishing conditions that apply small loads
3. Uniformity across the wafer surface

Note that both 1 and 2 are closely related to the quality of wafer planarization as well as polishing efficiency, as well as 3. Although an extensive care must be taken as a load is applied to the wafer, forming some sort of grooves onto the polishing pad is considered to be one of the countermeasures against wafer edge exclusion.

2.3 Requirements of polishing pad and conditioning treatment

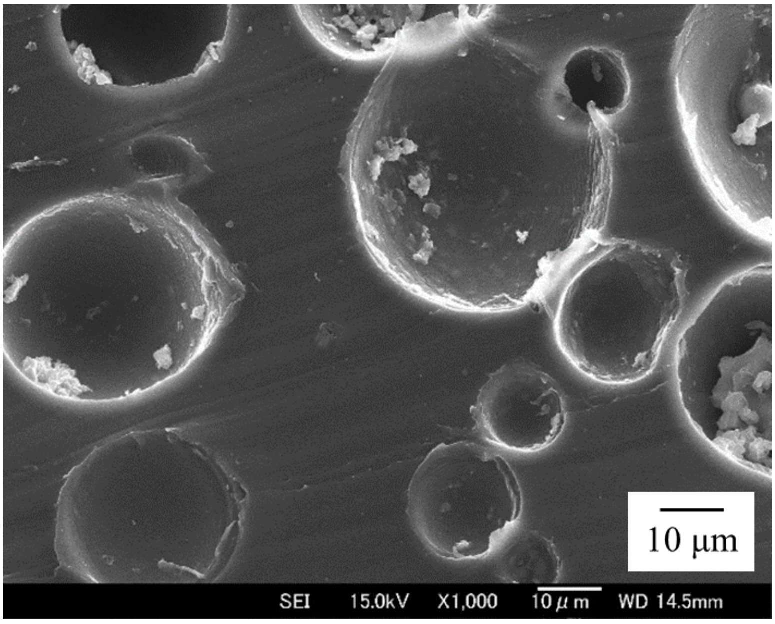
The elastic deformation of polishing pads is of great importance considering the behavior of a polishing pad. It is necessary to select the materials of polishing pad based on the hardness and thickness regarding elastic deformation as well as the thickness variation of the entire polishing pad. The following represent the fundamental requirements of the polishing pad in the CMP.

It is necessary for the polishing pad to:

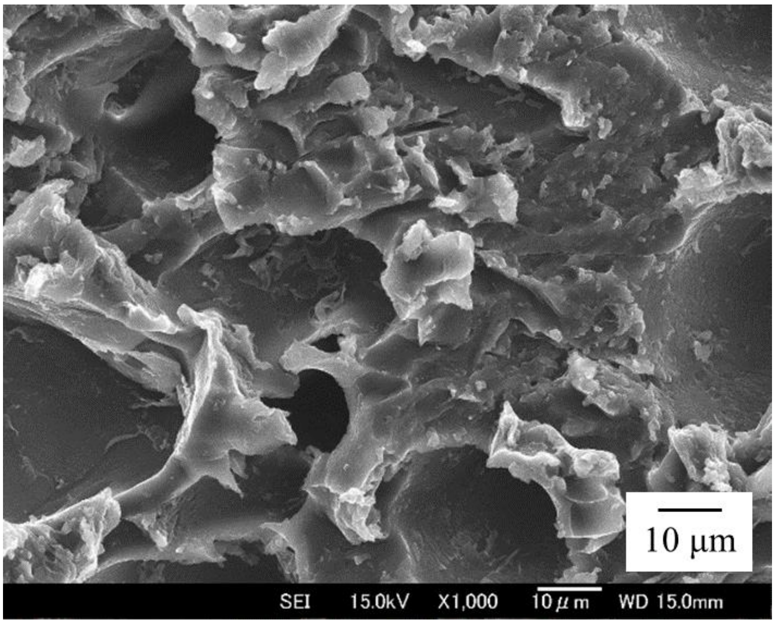
1. retain the slurry,
2. have enough rigidity to prevent permanent deformations,
3. ensure the uniformity of the wafer,
4. ensure repeatability, or contain a structure to extract debris, and
5. contain little impure material.

As to 1, since it is necessary for the slurry to flow underneath the wafer so as to polish the surface, retaining slurry is imperative. Most polishing pads contain patterned grooves with small pores which also play a role in extracting debris as referred in 4. Furthermore, the grooves on the polishing pad surface also contribute to attaining a good flatness of the wafer due to the improved load distribution. As for 3 and 5, the thickness and cross-sectional structure of the polishing pad stand in a trade-off relationship. Lastly, as for 2, in order to introduce CMP to the semiconductor processes, thorough considerations are required for improving the purity and quality management of the material used in polishing pads along with the improvement of the purity of slurries.

Since most polishing pads come with miniscule pores and grooves on the surface, debris or remnants of chemical reactants will be trapped by them, thereby deteriorating the polishing efficiency as shown in Figure 2.3. Once the pores and grooves on a polishing pad are blocked, it becomes difficult to extract the debris so the polishing pad surface goes back to its initial condition. Thus, conditioning treatment is implemented in which the blocked surface is removed with diamond grains [13-16]. The conditioner holds diamond grains which are electrodeposited. The conditioner used in the experiments is shown in Figure 2.4. As a result, by removing the polishing pad surface which is clogged, a new layer underneath the clogged surface replaces the latter, rendering the polishing pad as good as the initial state of the polishing pad. Hence, in order to maintain a polishing efficiency that is stable and repeatable, the surface structure as well as the cross sectional structure must be uniform [17].



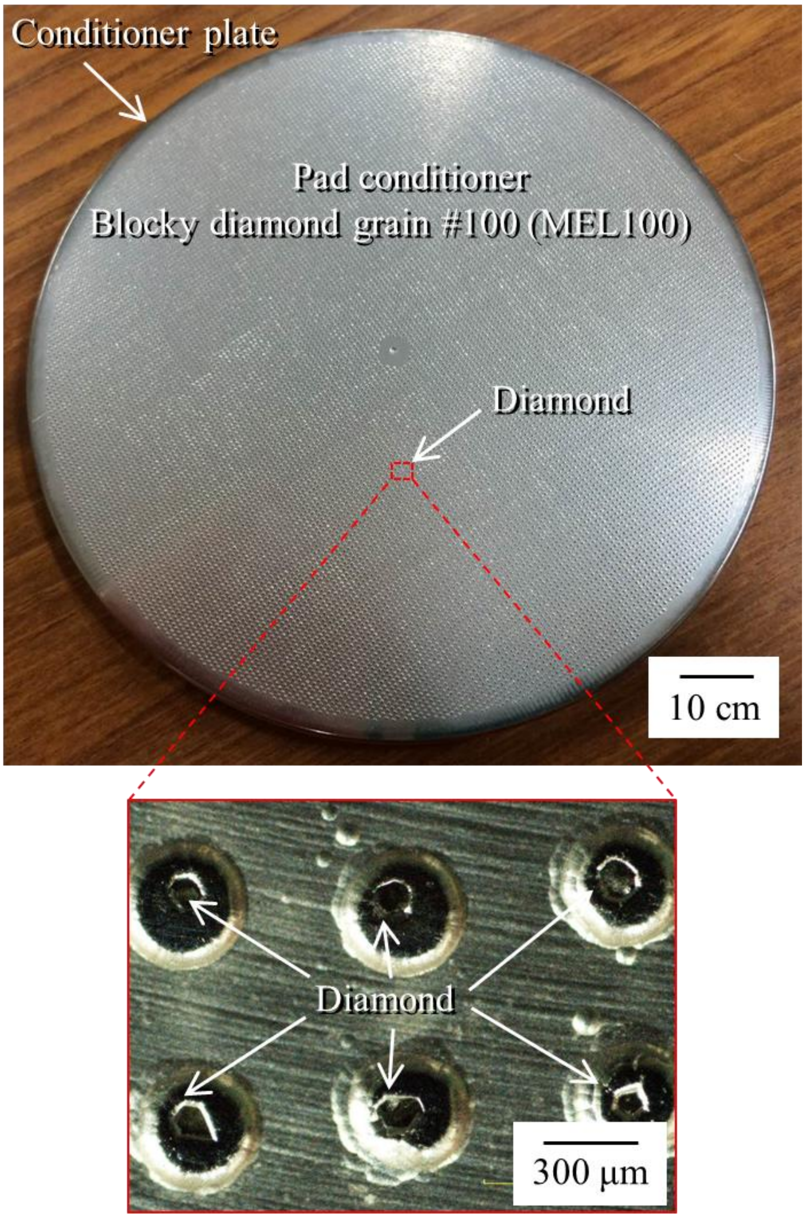
(a) Before break-in



(b) After break-in or conditioning treatment

Figure 2.3: Polishing pad surface (a) before break-in, and (b) after break-in or conditioning treatment

(a) With blocky diamond grains #100



(b) A microscopic image of diamond grains

Figure 2.4: Pad conditioner (a) with blocky diamond grains #100, and (b) a microscopic image of diamond grains

Figure 2.5 depicts the transition of a polishing pad surface during the CMP. Note that the asperity represents the structures of a polishing pad surface such as grooves and pores which influence the polishing efficiency. Conditioning treatment is required for CMP process [18-21].

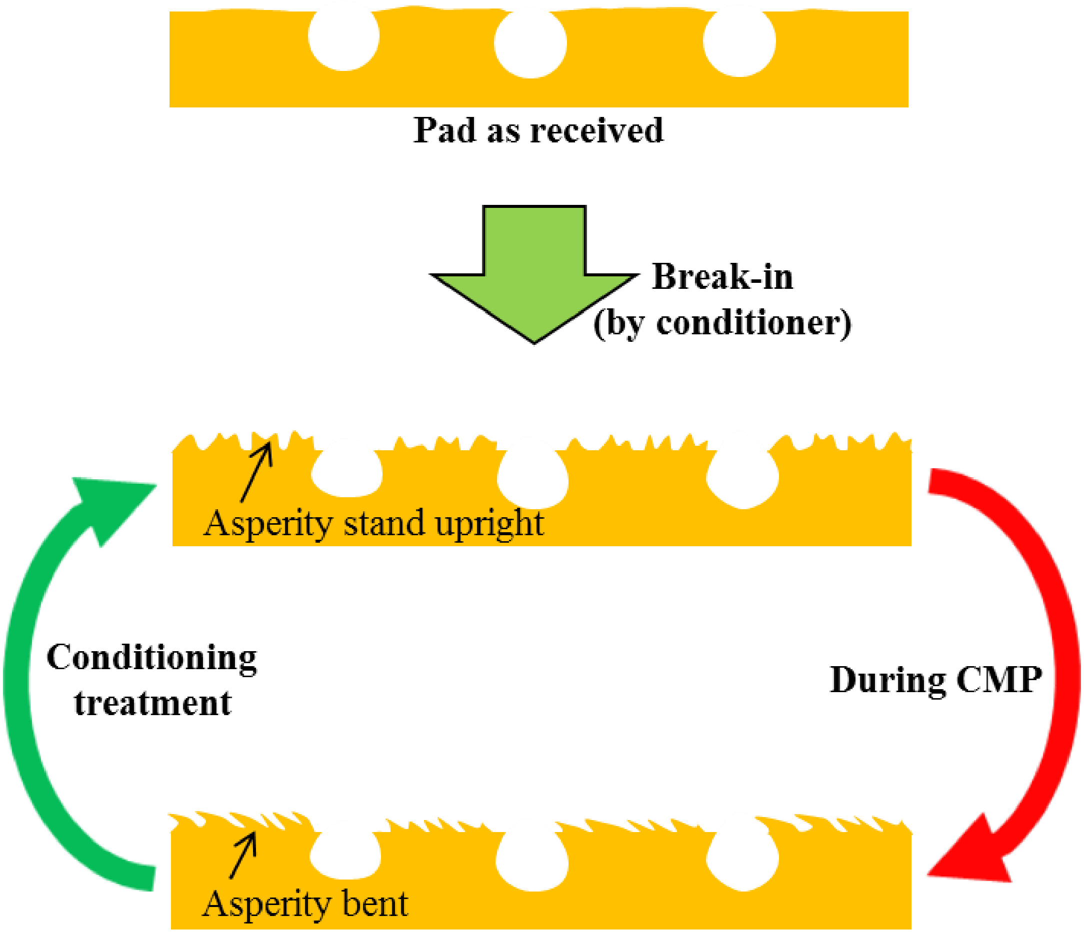


Figure 2.5: Polishing pad surface cycle during CMP process

Polishing pads are vastly categorized into 2 types; namely, polishing pads with and without perforation. Furthermore, perforated polishing pads are categorized into independently and continually perforated polishing pads as shown in Figure 2.6.

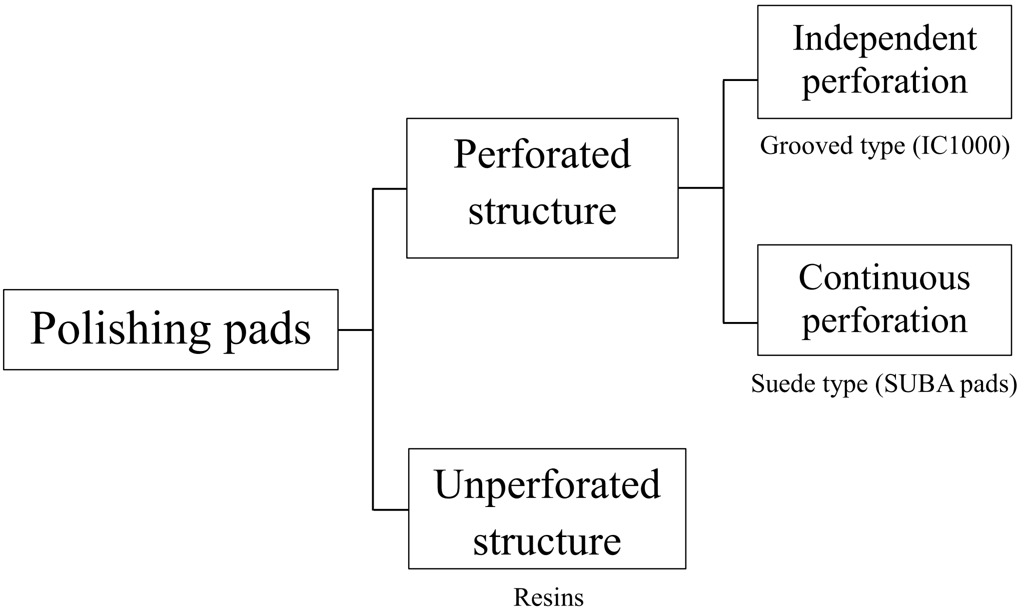


Figure 2.6: Categorization of polishing pads

Independently perforated polishing pads have several advantages such as the conservation of slurry in that the slurry stays between the wafer and polishing pad or the contacting area without sinking inside the polishing pad. However, blockages of the polishing pad surface are more frequent for the slurry that does not soak underneath the polishing pad surface, and debris and reactants block the pores on the surface. Therefore it is necessary to beef up the slurry flow rate and construct grooves so as to extract debris more efficiently. Moreover, implementing conditioning on a regular basis helps stabilize the MRR, improve the wafer surface quality, and increase the polishing pad life.

Continually perforated polishing pads are made from suede as the basic material, which contains different kinds of resins and the structure indicates continual perforation. Based on typical polyester suede, continually perforated polishing pads are capable of achieving high MRR and a smaller amount of wafer edge exclusion; hence they are often used in the earlier stages of polishing process which include the polishing of bare silicon wafers. Furthermore, owning to the concave structure on the surface of continually perforated polishing pads, which is called the nap layer with a diameter of several hundred microns, the slurry is retained in the layer preventing scratches on the wafer, also achieving a quality wafer surface. For this reason, continually perforated polishing pads are also used post CMP cleaning.

Combining the merits of continually and independently perforated polishing pads, 2 layered, or composite polishing pads are effective to satisfy the trade-off relationship between planarity and uniformity. The surface of polishing pad needs to have as few bumps as possible excluding the perforation in order to retain the slurry. Figure 2.7 shows the surface image of one of the most commonly used 2 layered polishing pads, IC1000/SUBA400 pad [17, 21]. The Polishing pad IC1000 is used in the experiment.

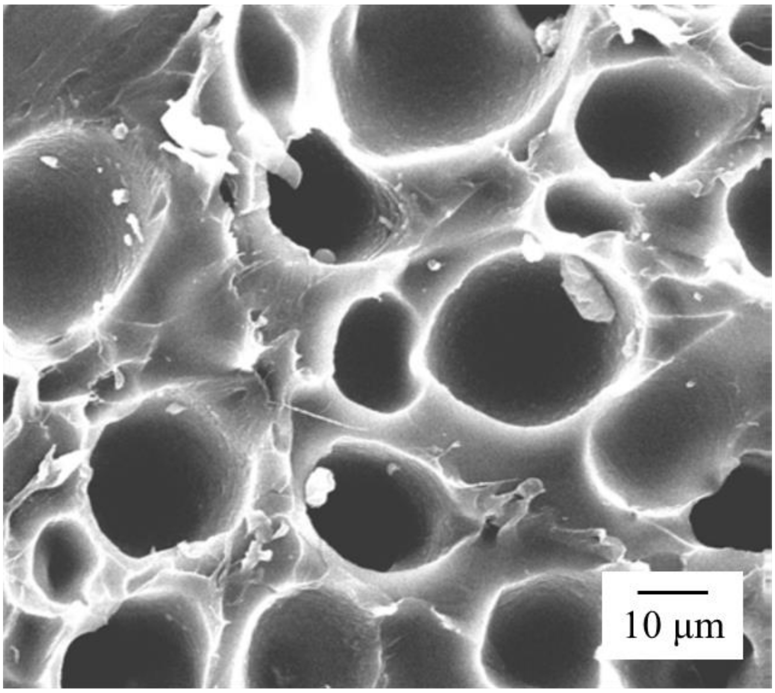


Figure 2.7: Image of IC1000 polyurethane based polishing pad

2.4 Carrier/Platen rotational direction and speed

Due to the complex interaction of the slurry, carrier, and polishing pad in CMP, the complete picture of CMP mechanism is yet to be known. However, the non-uniformity of large wafers caused by uneven slurry flow distributions or the shortage of slurry supply underneath the wafer may be improved by adapting varied platen/carrier rotational speed. In several cases, it is reported that the uniformity of a wafer with a diameter of 200 mm was improved by setting platen/carrier speed to be 50/60. However, this method is occasionally taken and is derived from the experience of engineers. It is reported that MRR is inversely proportional to the slurry film thickness between the wafer and polishing pad [22, 23]. Therefore, the reversed rotation of platen/carrier is likely to result in a thinner slurry film, hence a higher MRR. In this report, the Variable Rotational Polishing method or VRP method is proposed in which the time-dependent rotational speed of platen produces a thinner slurry film compared to the conventional CMP method in which the rotational directions of platen and carrier are the same.

2.5 Study objectives

The Chemical Mechanical Polishing technology plays a tremendous role in the semiconductor industry and has developed as the shrinkage of device was realized, which made electronic device process faster and store larger amounts of information. As the demand in the electronics market increases, engineers will face a number of problems including the improvement of throughput, although an increased throughput means a decreased price in the market. Throughputs can be enhanced by enlarging the wafer size, which in turn, raises issues concerning the CMP process such as the shortage of slurry supply underneath the wafer. Although the relationship between the behavior of slurry and the MRR has room for further inquiries, on a macroscopic scale, the flow path of slurry is seen as depicted in Figure 2.8, in which the slurry is provided near the center of the polishing pad. The slurry is retained by the polishing pad which is rotating; therefore, it will flow underneath the rotating wafer in time. Despite the polishing parameters such as slurry flow rate and the rotational speed of the carrier and platen, a larger wafer is more likely to cause the shortage of slurry to supply underneath the wafer, which causes several defects including scratching in detriment of the construction of multilevel interconnections as well as the throughput. Therefore, the correlation between polishing pad surface, slurry flow path, and the MRR is also of great importance.

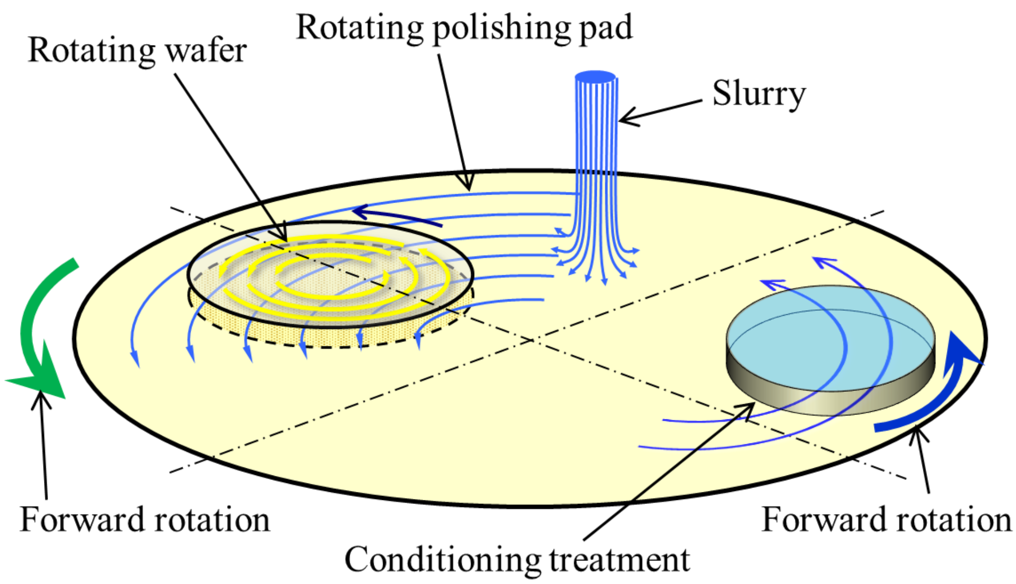


Figure 2.8: Typical flow path of slurry on the polishing pad

Lastly, reducing the number of conditioning during the CMP process to a small extent contributes to gaining a higher throughput. This can be achieved by preventing the MRR from decreasing in the CMP. The study objectives are summarized as follows:

1. **Improved cost performance in the CMP process**
   To increase of the material removal rate (MRR) by Variable Rotation Polishing (VRP) method

2. **Polishing pad surface topology and slurry flow distribution vs MRR**

3. **Sustainment of MRR during CMP with a reduced number of conditioning**
   To evaluation of dominant parameter to sustain the material removal rate (MRR)

In order to achieve our goals, Variable Rotational Polishing method, in which the platen rotates in the opposite direction to the carrier, was implemented which in turn was compared with the conventional CMP method (called as Conventional polishing in this dissertation) in order to discuss the validity and mechanism of VRP method.

Chapter 3

The Variable Rotation Polishing Method in the CMP Process

3.1 Concept of the Variable Rotation Polishing method

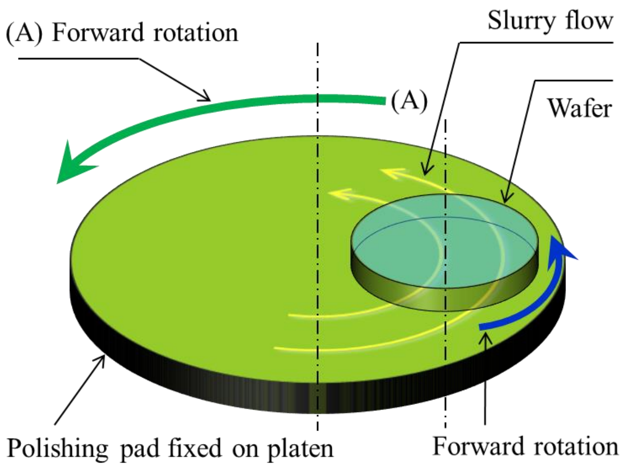
This dissertation aims at studying the issue concerning the slurry supply around the center area of the platen applying the Variable Rotation Polishing (VRP) method in the CMP process. Comparatively high material removal rates were found from the experiment changing the backward rotation angle of the platen while the material removal mechanism during CMP is in veil yet.

In the case of the conventional CMP tool, the slurry may be unable to fill in the narrow gap between wafer and polishing pad around the center area when the wafer size becomes larger [10], and the slurry costs become prohibitive due to the increase of the pad area. In this study, the

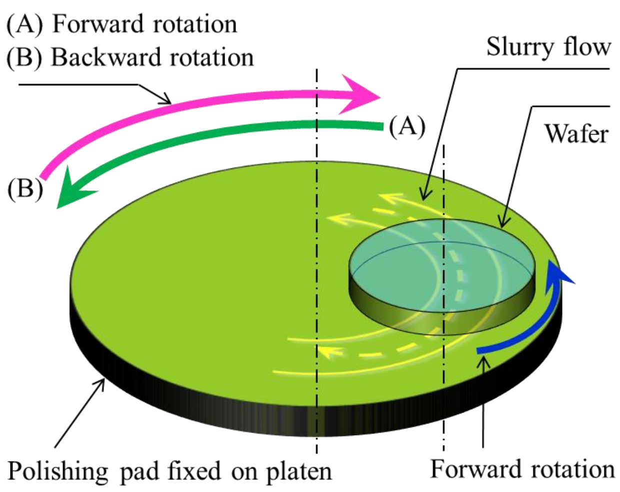
Variable Rotation Polishing method is proposed in order to increase the slurry flow efficiency in the CMP process for increasing polishing efficiency, resulted from the unsteady slurry which flows into the center of wafer sufficiently when the wafer becomes larger in size. The influence of the asperity on a polishing pad was investigated to increase the material removal rate by implementing the VRP method although the rotational directions of the platen and polishing head in the case of the conventional rotation in CMP process are both counter clockwise preventing the slurry from filling around the center area of the wafer. In order to verify the proposed method, a control unit to vary platen rotation speed, rotation direction and rotation angle was experimentally developed.

For the material removal mechanism during the CMP process applied to wafer surface planarization in the semiconductor manufacturing, the material removal of wafer surface during CMP is conducted by the adhesion of the reacted silica layer of the SiO_2 substrate on the fine particles during attachment on the substrate surface on a microscopic level, and the unsteady slurry flow of the narrow gap between the wafer and the polishing pad [8, 11, 24]. The conventional polishing, in which the wafer carrier and the platen rotate in only one rotational direction throughout the polishing process, is shown in Figure 3.1(a). The VRP method is defined as bidirectional, forward and backward rotation, with variations of rotation angle and rotation speed, where the slurry finally returns to the wafer by backward rotation of the

VRP method in accordance with the concept of this dissertation. Thus, the VRP method could also save the consumption of slurry as shown in Figure 3.1(b).



(a) Conventional polishing



(b) Variable Rotation Polishing method

Figure 3.1: Concept of the polishing methods (a) Conventional polishing, and (b) Variable Rotation Polishing method

This method could improve the slurry flow distribution around the center area of the platen because the method efficiently causes the slurry to fill the area by backward rotation [25]. Constant signals for controlling the forward rotation only at 60 rpm were applied for the conventional polishing throughout the polishing time. On the other hand, the sine wave for forward and backward rotation was applied for the Variable Rotation Polishing method as shown in Figure 3.2, and both rotation angles were adjusted by time; $T_{forward}$ for forward rotation angle and $T_{backward}$ for backward rotation angle, as shown in Figure 3.3. The platen rotation in the case of the conventional polishing, forward rotation only for all the time is shown in Figure 3.4 from a top view and Figure 3.5 from a bird's eye view. On the other hand, the Variable Rotation Polishing method, forward rotation angle 360º at all conditions (step 1), and backward rotation angles set at 90º, 180º, 270º and 360º (step 2) movement for the platen at various polishing conditions are shown in Figure 3.6 from a top view and Figure 3.7 from a bird's eye view.

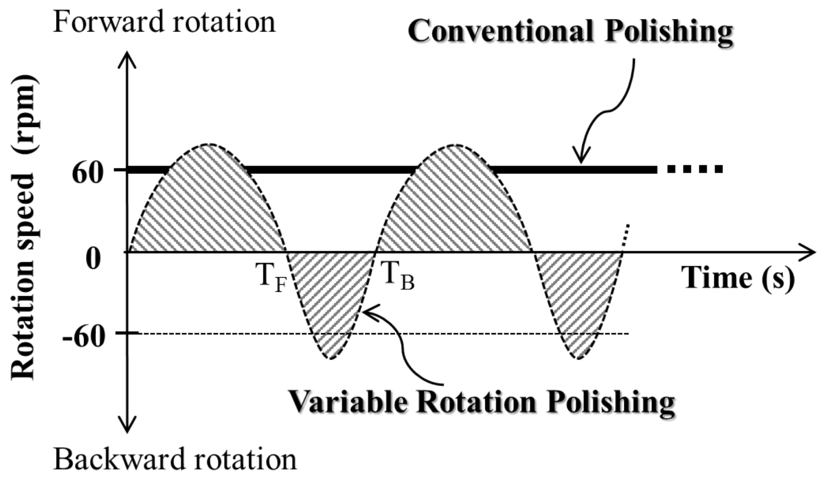


Figure 3.2: Rotation speed in variation of platen rotation over time from conventional polishing and Variable Rotation Polishing methods

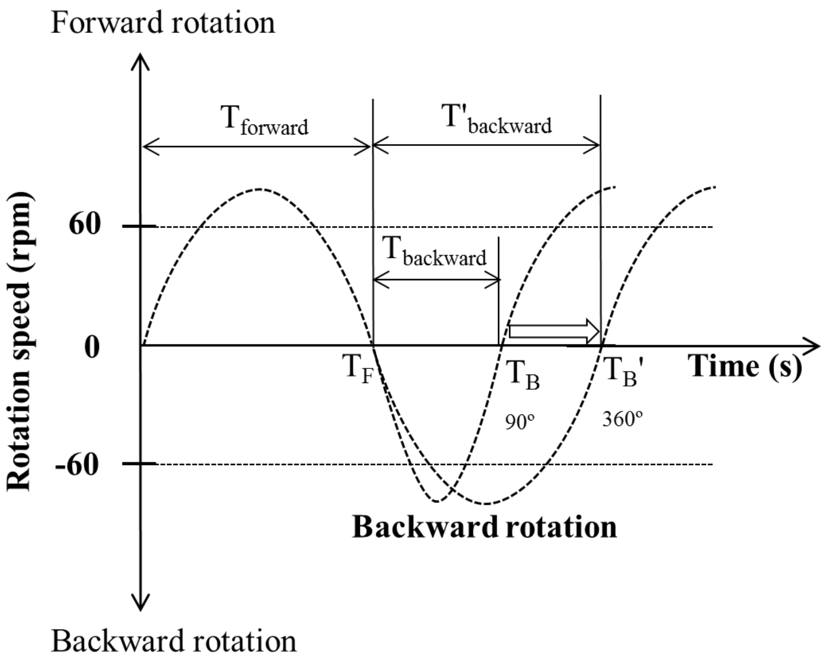


Figure 3.3: Control methods of backward angles from 90º to 360º adjusted by $T_{backward}$

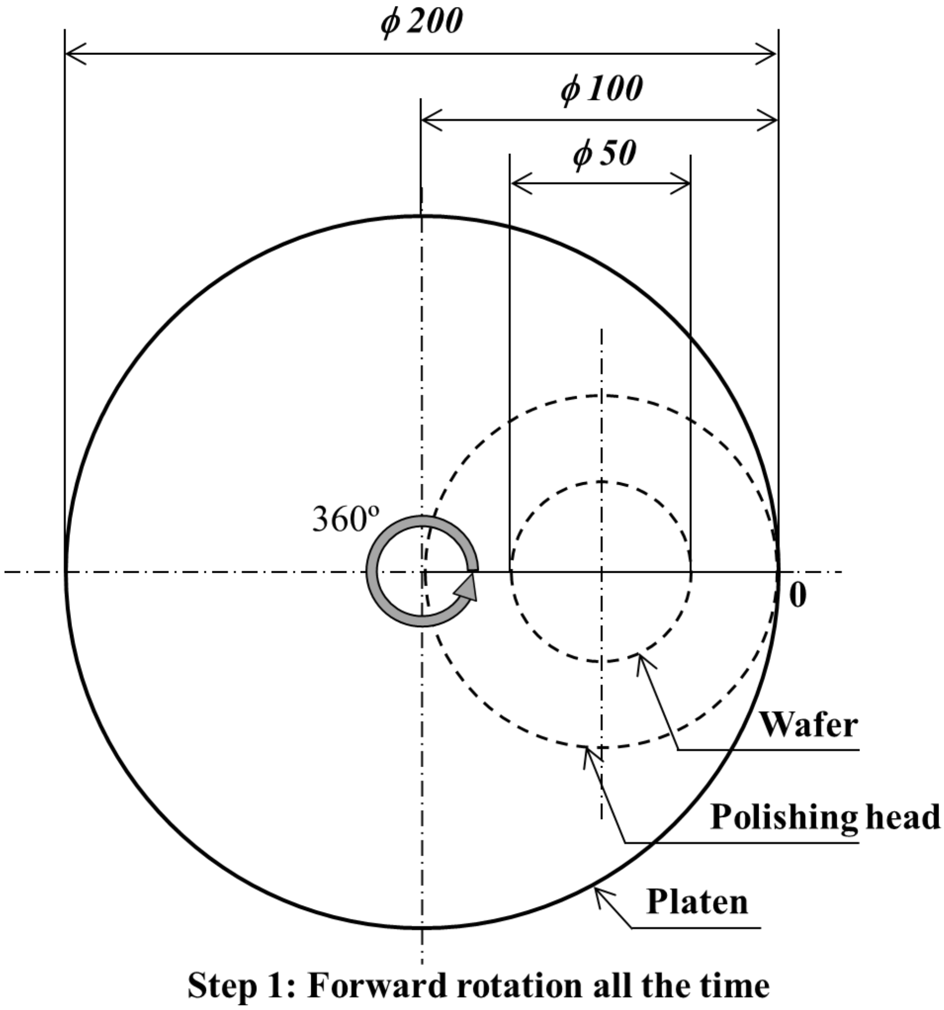


Figure 3.4: Conventional polishing, forward rotation all the time (top view)

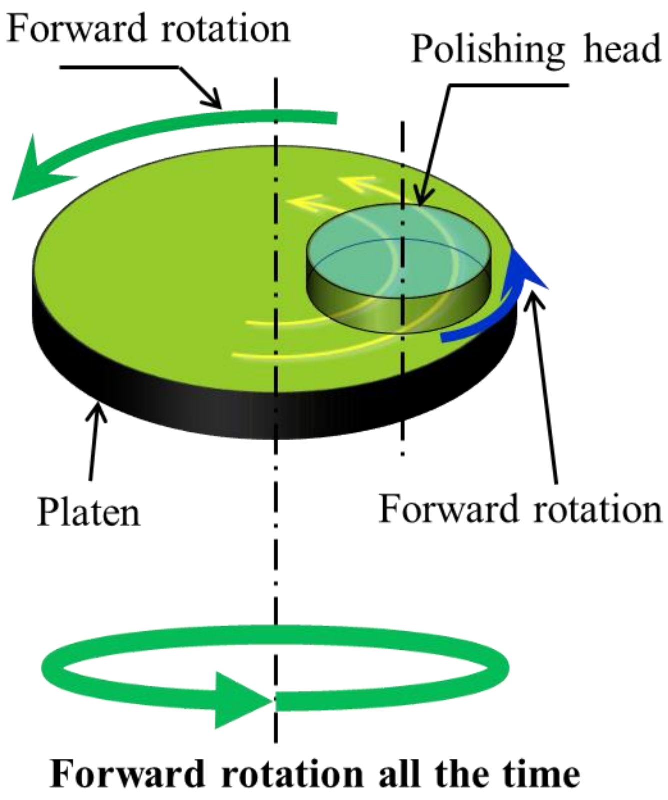


Figure 3.5: Conventional polishing, forward rotation all the time (bird's eye view).

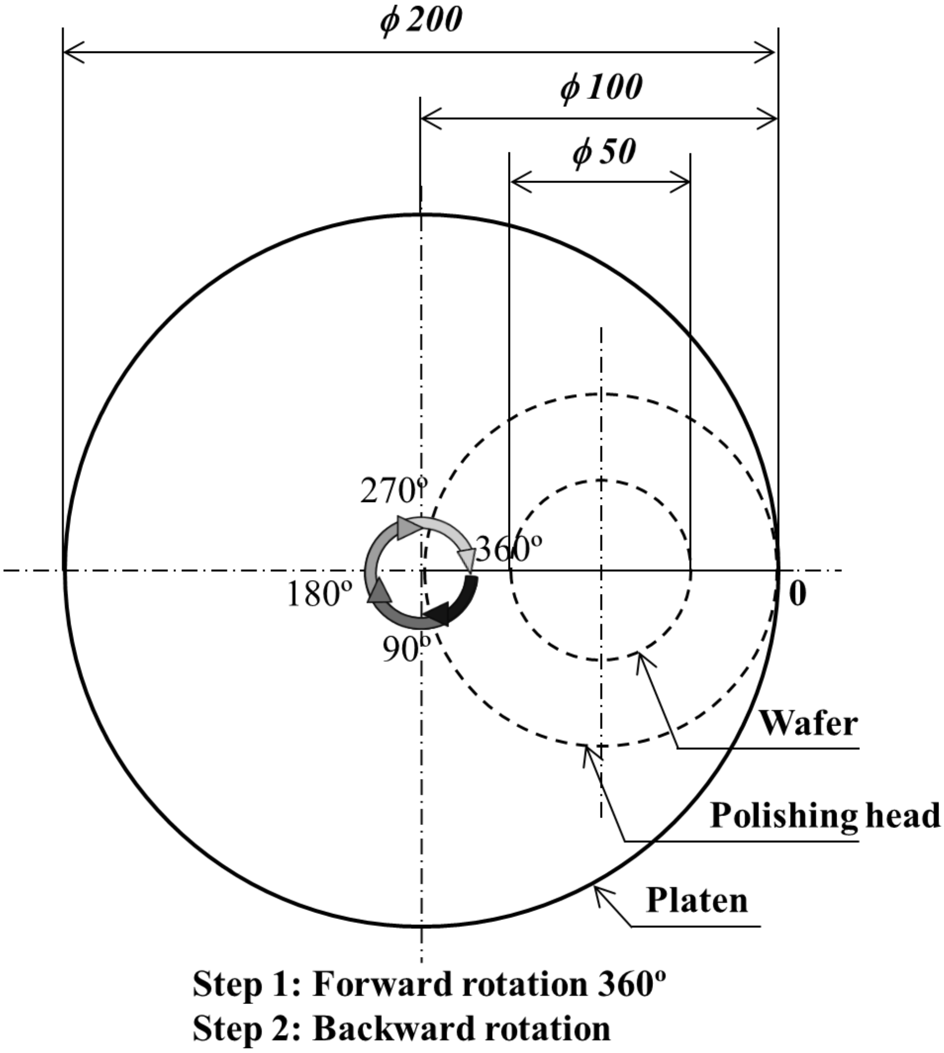


Figure 3.6: Variable Rotation Polishing method, forward rotation angle 360° in all the conditions (step 1 in Figure 3.4), and backward rotation angles set at 90°, 180°, 270° and 360° degrees (step 2) movement for the platen at various polishing conditions (top view)

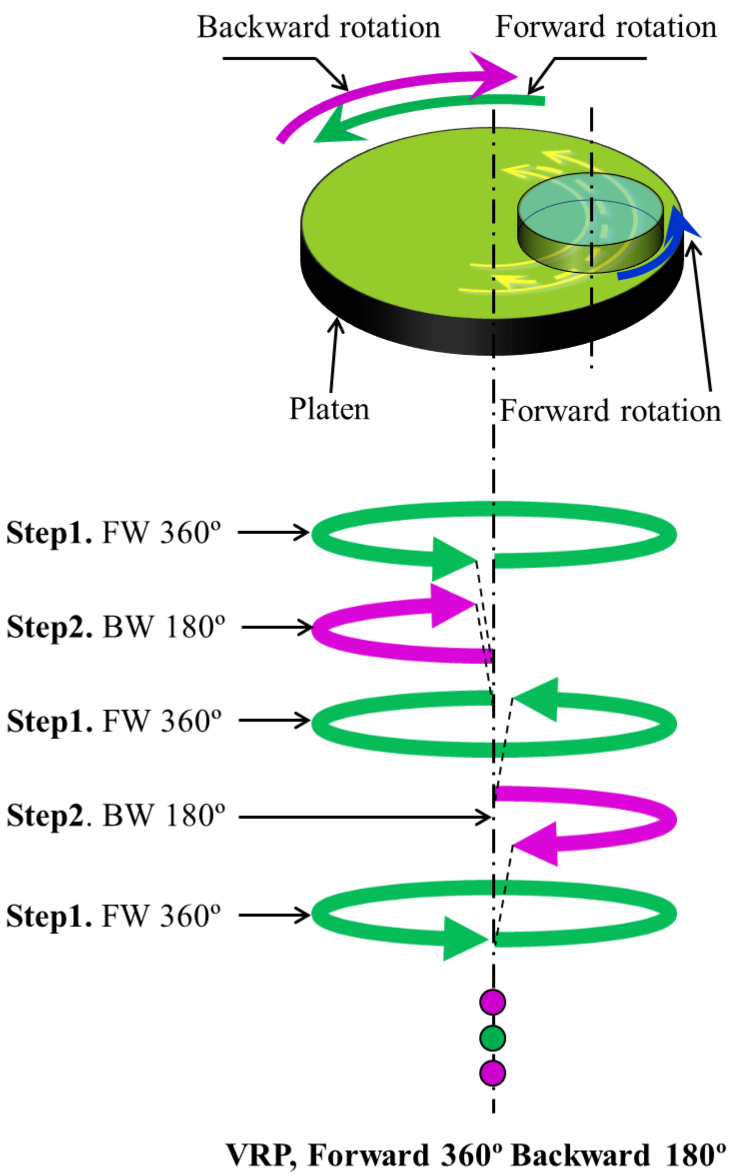


Figure 3.7: Variable Rotation Polishing method, forward rotation angle 360º in all the conditions (step 1 in Figure 3.4), and backward rotation angles set at 90º, 180º, 270º and 360º degrees (step 2) movement for the platen at various polishing conditions (bird's eye view)

3.2 Experimental methods

A polishing pad with 200 mm diameter was set on the experimentally developed platen of the Variable Rotation Polishing comprising the CMP polisher (Doctor-Lap) as shown in Figure 3.8. Figure 3.9 shows the experimental apparatus used for verifying the VRP method. The CMP experimental conditions are shown in Table 3.1 The experiment consists of five types of rotation. The *i* type was the conventional polishing with forward rotation only. The *ii* to *v* types with backward rotations of 90º, 180º, 270º, 360º were added, respectively.

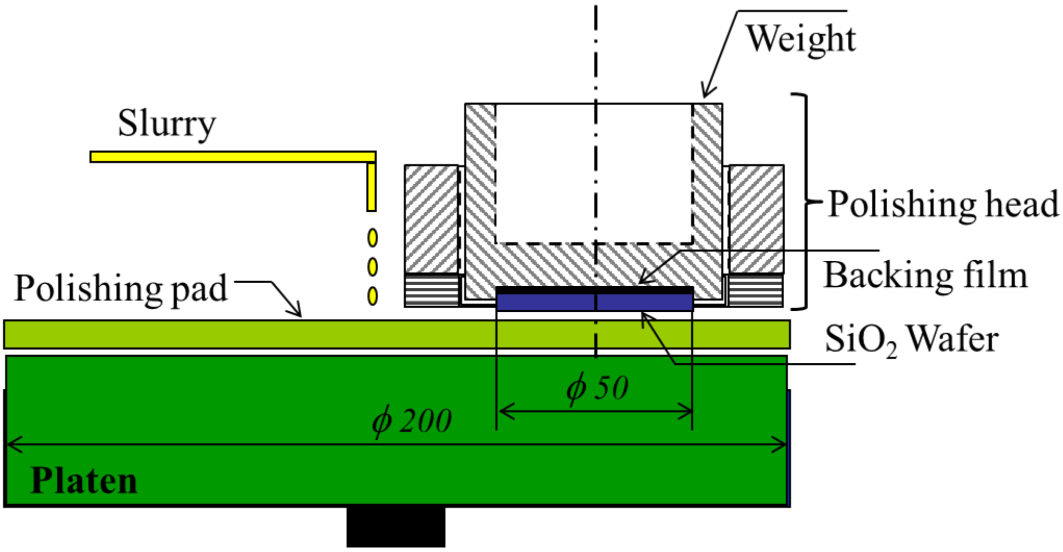


Figure 3.8: The structure of the CMP device where the polishing pressure is adjusted by weight.

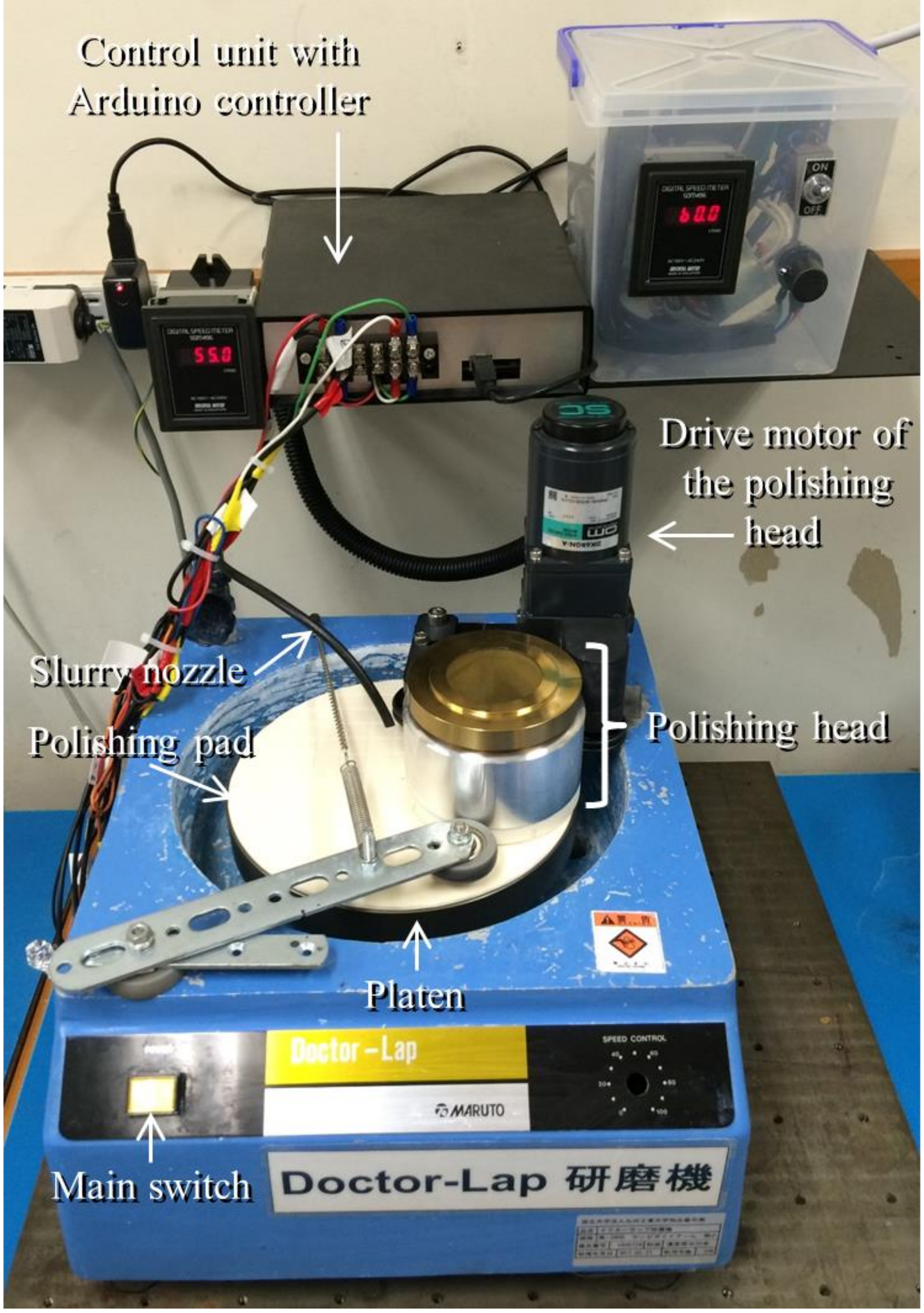


Figure 3.9: The experimental apparatus used for verifying the VRP method

Table 3.1: CMP experimental conditions

Silicon substrate	• ϕ 50 mm $t = 0.725 \pm 0.025$ mm • SiO_2 film (1,500 nm) is deposited on the substrate
Backward rotation angles (Forward rotation angle is constant at all conditions)	*Type i* Backward 0˚ *Type ii* Backward 90˚ *Type iii* Backward 180˚ *Type iv* Backward 270˚ *Type v* Backward 360˚
Conditioning time	5 minutes
Polishing pad	• IC1000/Suba400 Nitta Haas Co., Ltd. • XY-Groove
Slurry	• SS 25 Cabot Microelectronics Co., Ltd. • pH 10.6 (KOH) • 12.5wt%
Conditioner of the polishing pad	• Mitsubishi diamond • Blocky diamond type (#100)
Polishing pressure	6.89 kPa (1 psi)
Polishing head and platen rotation speed	60 rpm (Average value)
Slurry flow rate	10 ml/min
Polishing time	2.5, 5, 7.5, 10 minutes

These were measured by the reflectometric interference spectroscope; TFW-100 Thin Film Analyzer Unit Lambda Vision Inc. Prior to each experimental polishing, the polishing pad (IC1000/Suba400 XY-Groove Nitta Haas Co.,Ltd.) was conditioned by Mitsubishi diamond blocky diamond type (#100) conditioner for 5 minutes with 26.6 N load, and the rotational speed of both platen and conditioner was 60 rpm.

3.3 Calculation of material removal rates

The material removals were evaluated by the difference of the silicon dioxide film thickness before and after CMP experiments. Each material removal value was averaged from the total 100 points, 25 points on each of 4 samples, as shown in Figure 3.10 and Figure 3.11 [26].

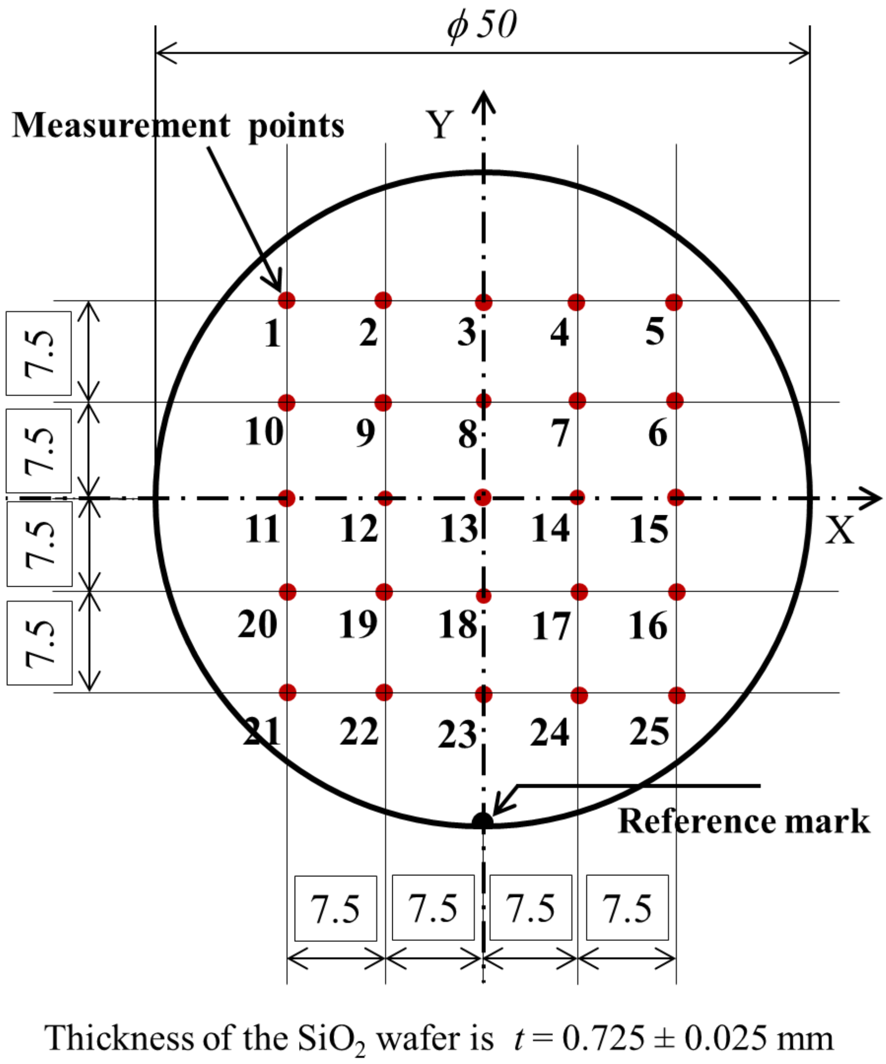
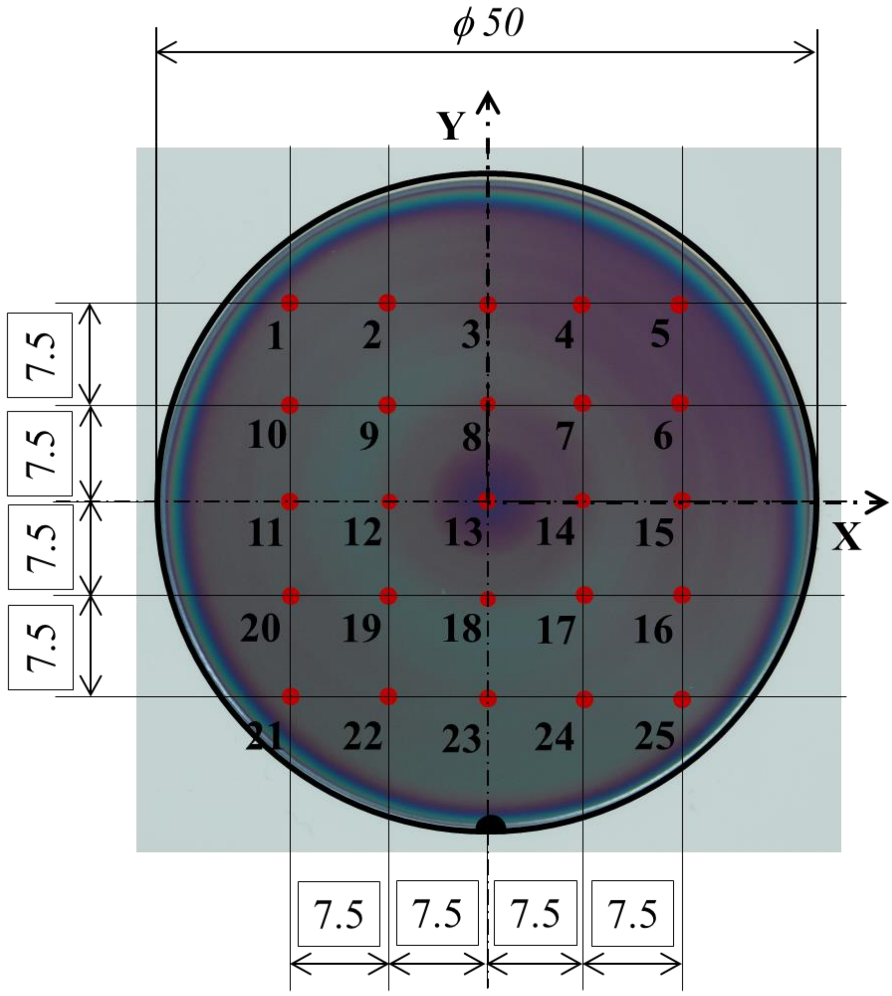


Figure 3.10: Measurement points to estimate material removal rates (MRR) of the CMP process



Thickness of the SiO_2 wafer is $t = 0.725 \pm 0.025$ mm

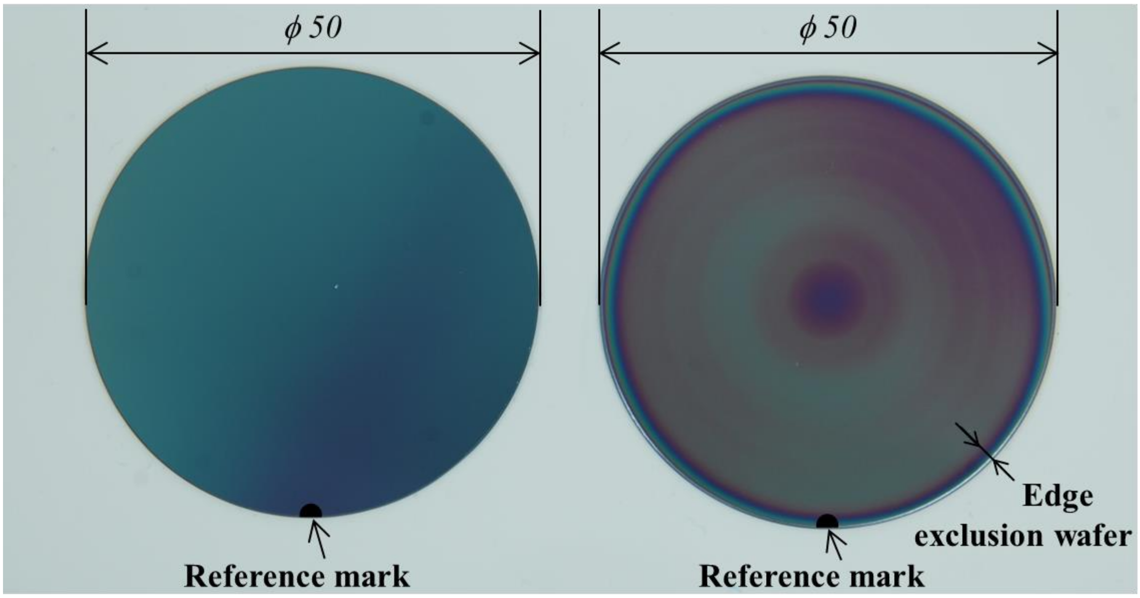
Figure 3.11: 25 measurement points are located within the area of allowable tolerance after wafer polishing

3.3.1 Methods of measuring and calculating the thickness of silicon dioxide films

1. Paste a polishing pad onto a platen.
2. Perform conditioning process (break in process) for the polishing pad.
3. Measure 25 points on the wafer before each CMP experiment as shown in Figure 3.12 (a).
4. Set the wafer to be polished into a carrier pocket.
5. Put the carrier to a retainer with loads.
6. Supply slurry to the center of polishing pad.
7. Rotate the platen and the carrier at the same time.
8. After the polishing is finished, clean the wafer and the polishing pad by pure water.
9. Measure the wafer at 25 points after CMP experiment as shown in Figure 3.12 (b).
10. Calculate the average thickness of silicon dioxide film from 25 points before and after the CMP experiment.

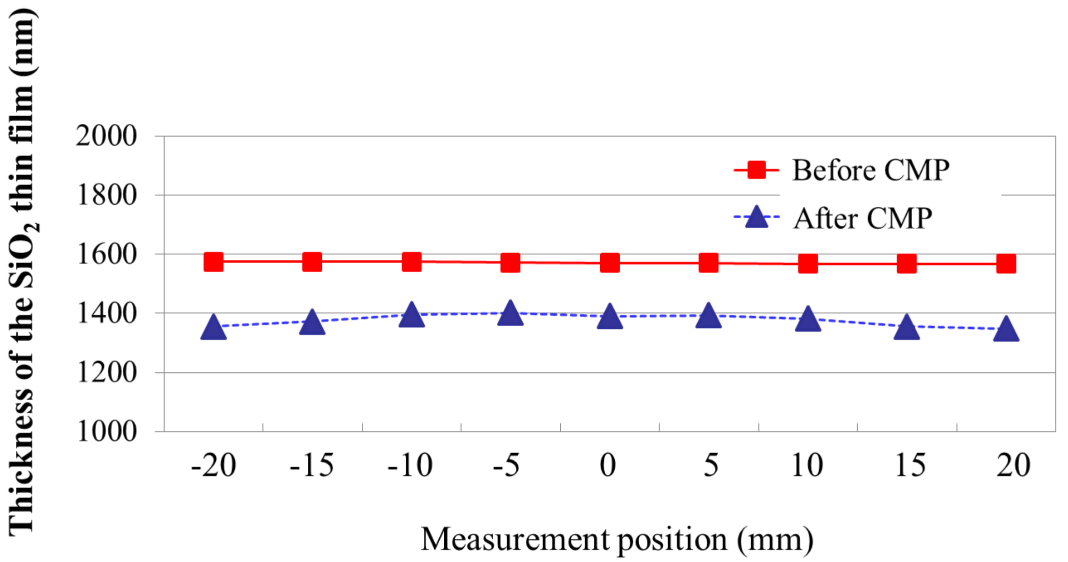
3.3.2 Material removal rate of the VRP method

The material removal rate is the difference between the thickness values of wafer before and after CMP experiment divided by the polishing time. Figures 3.13 (a) and (b) show the wafers before and after polishing, respectively. The diameter of the wafers is 50 mm. The wafers were cut using a wafer cutting tool.

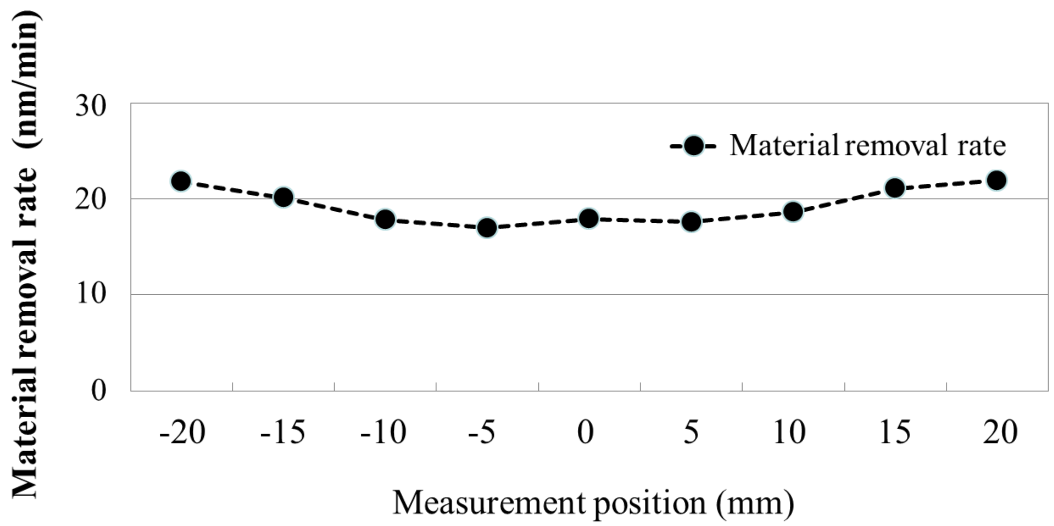


(a) Before CMP experiment (b) After CMP experiment

Figure 3.12: Silicon wafer (a) before CMP experiment, and (b) after CMP experiment.



(a) Thickness of SiO_2 films before and after the CMP experiment



(b) Material removal rate

Figure 3.13: Material removal rate of the VRP method (Polishing time 10 min, pressure on wafer 6.89 kPa or 1 psi) (a) thickness of SiO_2 films before and after the CMP experiment, and (b) material removal rate

3.4 Modifications of the CMP polisher

The Variable Rotation characteristics were realized by replacing the CMP polisher's platen motor with a DC controlled motor. The flowchart of the modified steps is shown in Figure 3.14.

(a) Initial specification of the Doctor-Lap

The motor speed is controlled by variable resistance (0-180 rpm). Originally, the Doctor Lap had forward rotation only as shown in Figure 3.15.

(b) VRP driving system version I

Motor speed is controlled by variable resistance (0-180 rpm). Motor direction is controlled by the circle plate as shown in Figure 3.16. Forward and backward rotations can be realized due to the modification. However, since the motor speed is fixed, the accuracy of forward and backward angles by the circle plate is low, and changing direction is not carried out smoothly. The VRP driving system required further improvement.

(c) VRP driving system version II

Motor speed is controlled by a function generator. Motor direction is controlled by the electronic circuit as shown in Figure 3.17. Figure 3.18 shows the appearance of the VRP driving system version II. This version can realize forward and backward rotations. Motor speed is represented by the sine wave (CHA output of function generator) and the accuracy of forward and backward angles by electronic circuit with output from CHB of function generator, with an improvement. Changing direction is carried out smoothly. Although initially CHA and CHB were in phase, the phase difference was seen later on. The VRP driving system required further improvement.

(d) VRP driving system version III

Motor speed and direction are controlled by Arduino controller as shown in Figure 3.19. Figure 3.20 shows the appearance of the VRP driving system version III. This version can achieve forward and backward rotations. Motor speed is represented by the sine wave from Arduino controller and the accuracy of forward and backward angles by Arduino controller is very good. Motor direction is controlled by the signal from Arduino controller between FW (forward rotation) using input port 3 and BW (backward rotation) using input port 4 alternatively. Motor rotation angles are determined by the duration in which signals are sent to either FW input or BW input. In this version, both signals for speed and direction are constantly in phase. Then the VRP driving system is selected for the experiment.

Figure 3.21 shows motor system inside the Doctor-Lap (CMP polisher) and Figure 3.22 shows all parts inside the Doctor lap before modification.

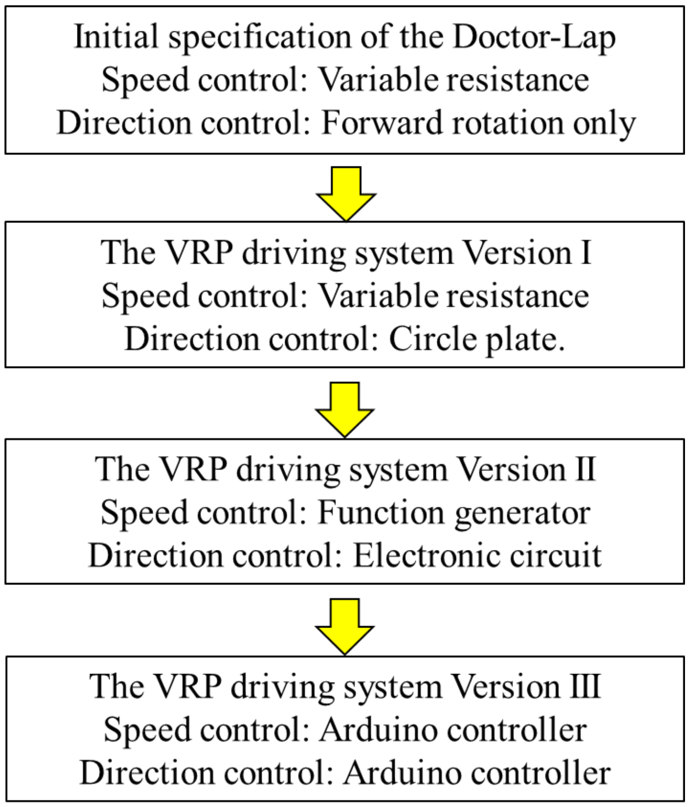


Figure 3.14: Flowchart of the modified steps of CMP polisher

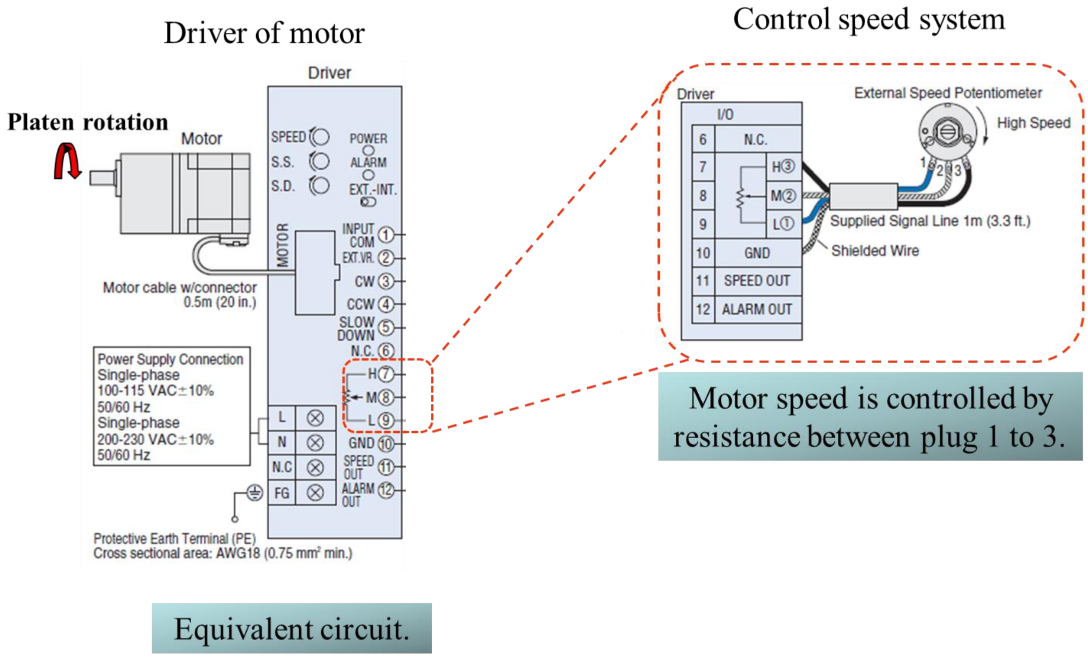
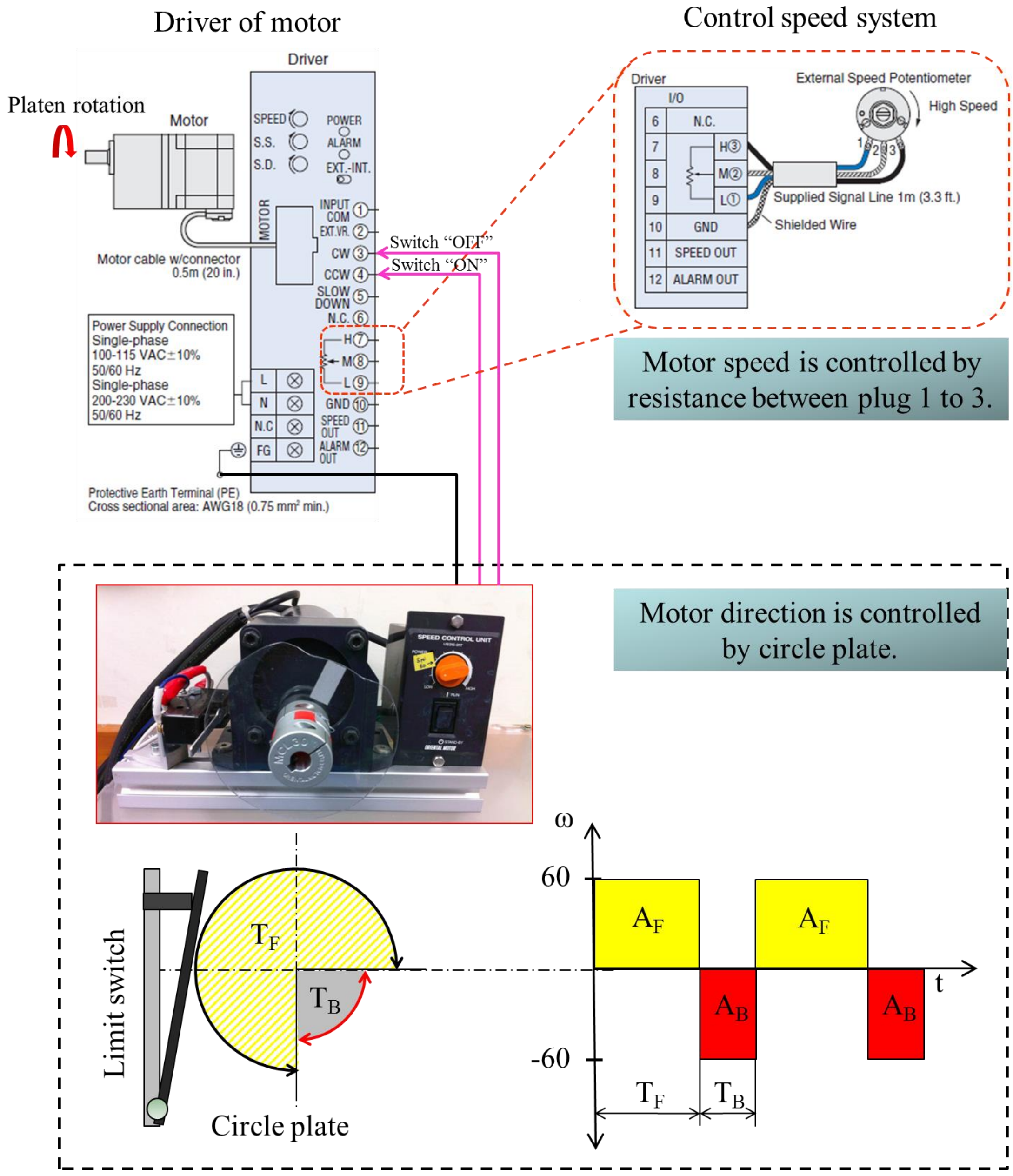


Figure 3.15: Block diagram of the control system of the initial specification of Doctor-Lap



The additional system to control forward and backward rotation.

Figure 3.16: Block diagram of the VRP driving system version I

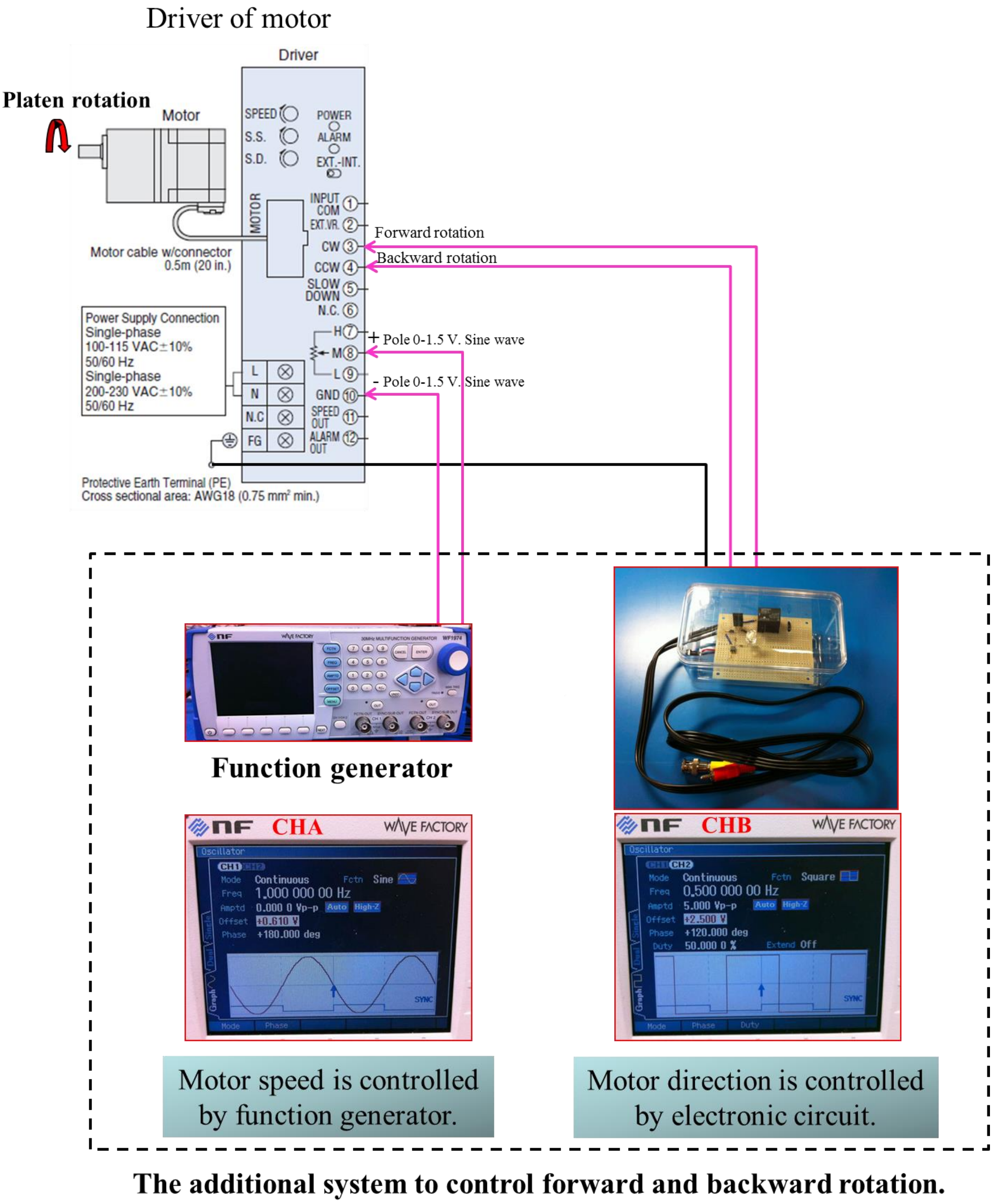
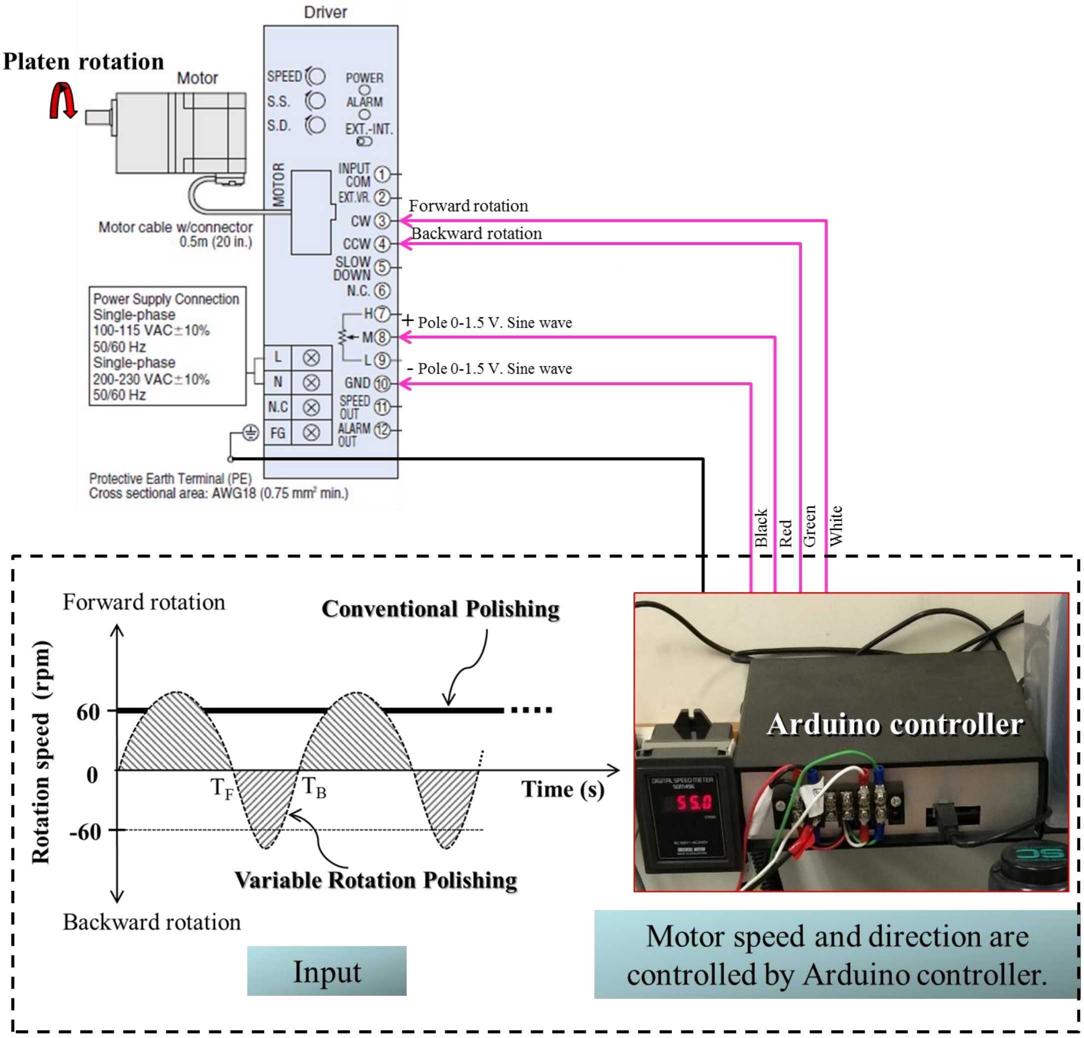


Figure 3.17: Block diagram of the VRP driving system version II

Figure 3.18: Appearance of the VRP driving system version II



The additional system to control forward and backward rotation.

Figure 3.19: Block diagram of the VRP driving system version III

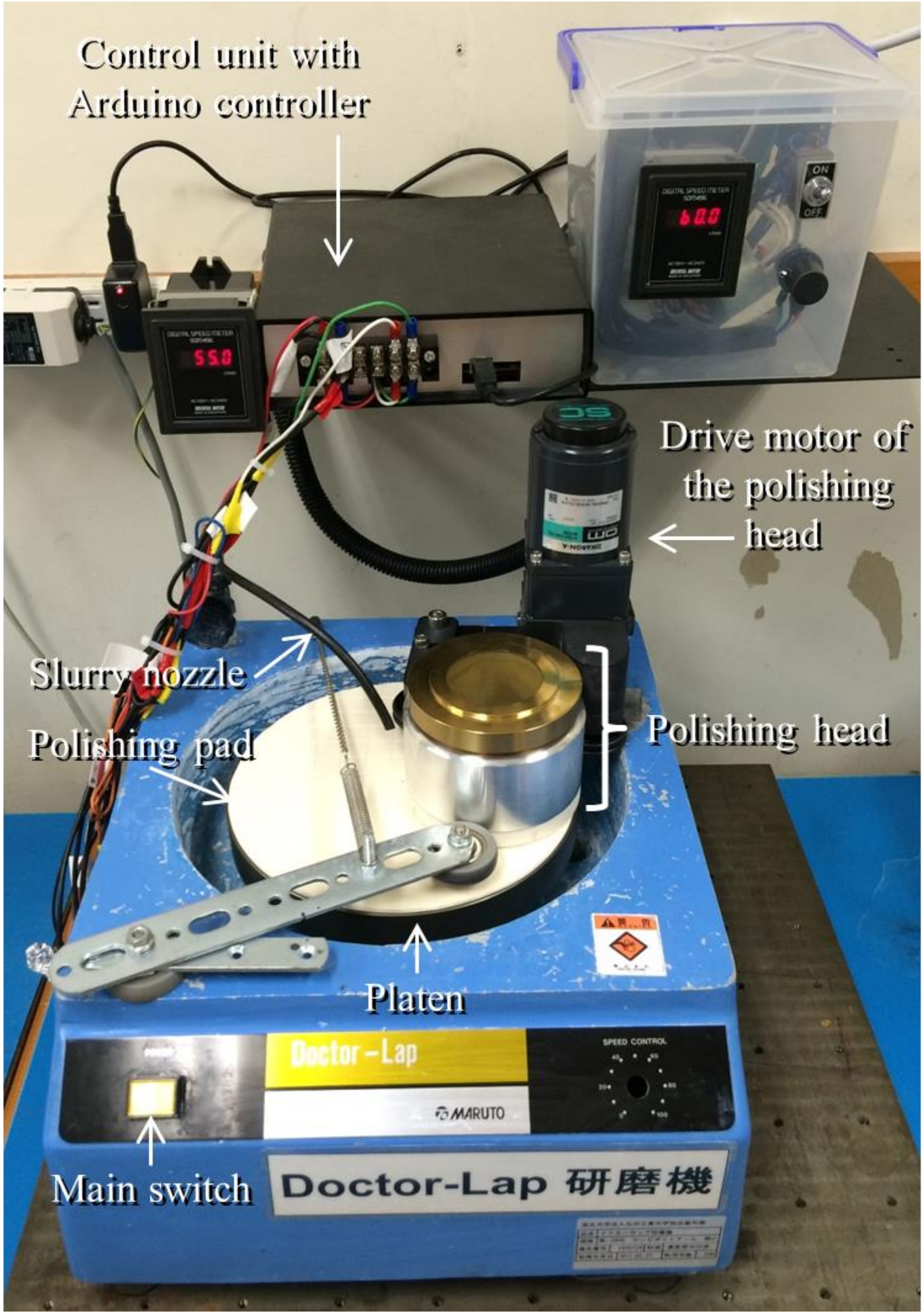


Figure 3.20: Appearance of the VRP driving system version III

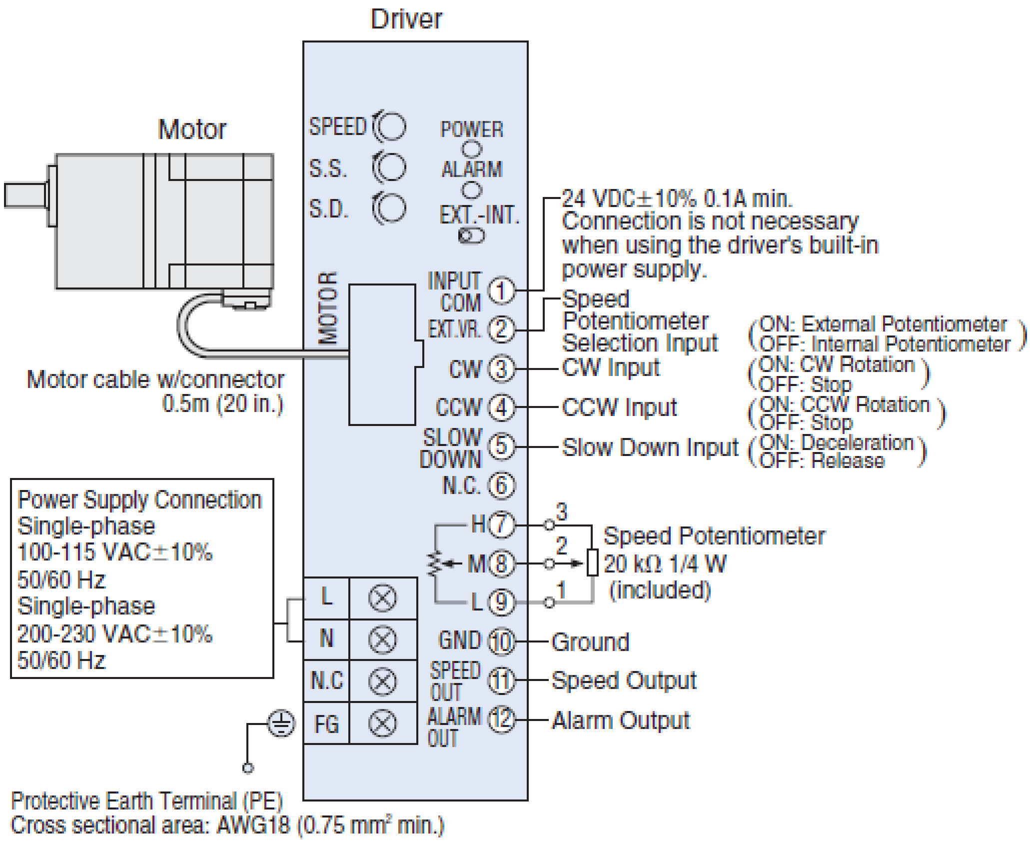


Figure 3.21: Block diagram of motor system inside the Doctor-Lap

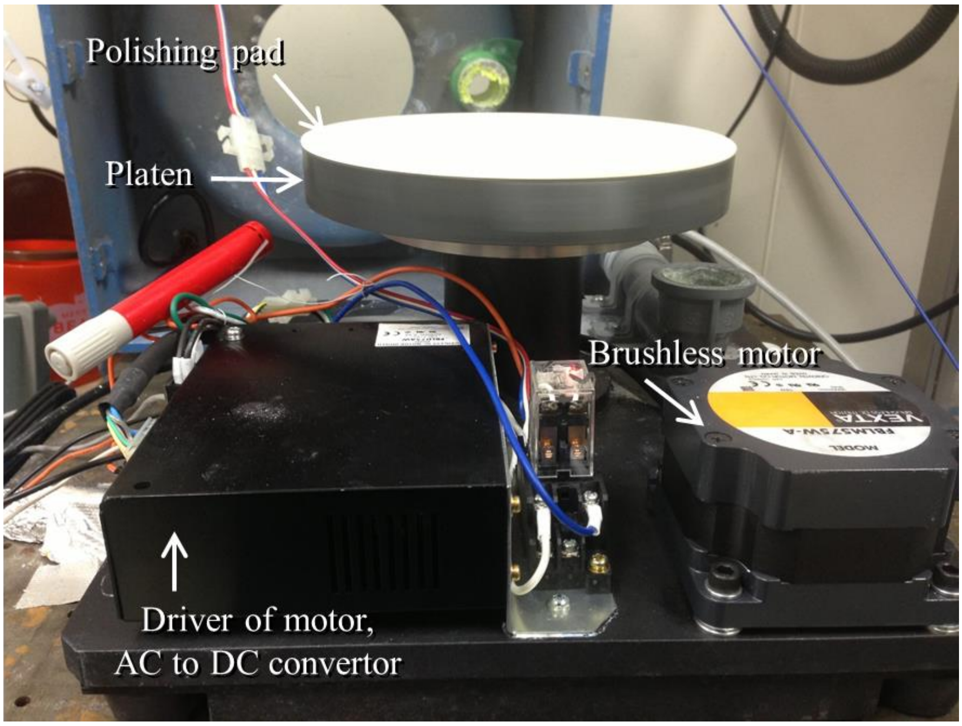


Figure 3.22: Photograph inside the Doctor-Lap

3.5 Summary

The VRP driving system version III was selected for all the experiments. Since the motor speed and direction are controlled with an Arduino controller, the accuracy of forward and backward angles are very good. Additionally, both signals for speed and direction from this version are constantly in phase. The forward and backward angles with loads and without loads are examined. The result shows that the error of forward and backward rotation angles is less than 5%.

Chapter 4

The Polishing Performance of Variable Rotation Polishing Method

4.1 Introduction

The CMP process is an essential step of metal and dielectric planarization in multilayer microelectronic device fabrication. In the CMP process, it is necessary to minimize the extent of surface defect formation while maintaining good planarity and optimal material removal rate [27].

The CMP process has emerged in the last two decades and grown rapidly as a basic technology and is widely used in semiconductor device fabrication because of its excellent planarization capacity. The CMP process is composed of a rotating table, a polishing head, a pad and slurry.

The CMP process takes place when the wafer surface is moved across the pad, under pressure and in the presence of slurry. The mechanical motion and down force are applied to the wafer by the polishing machine. The pad surface provides the rough points, or asperities, which makes contact with the wafer. The slurry provides the abrasive particles and the appropriate chemistry for the CMP process to proceed [28].

This chapter explains the polishing performance of the Variable Rotation Polishing method by evaluating the material removal rate (MRR) for the conventional polishing and the Variable Rotation Polishing method.

4.2 Polishing performance method

The removed thickness of the SiO_2 films in each rotation type corresponding to 2.5, 5, 7.5 and 10 minutes of polishing time were evaluated in the conventional polishing and VRP method. The material removals of the VRP method were higher than those of the conventional polishing due to the results calculated using the least squares method, [29] as shown in Figure 4.1. Figure 4.2 shows the dependence of the backward angles on the material removal rates for the 10-minute polishing time. Particularly, the material removal rate of the 360 degrees backward rotation in the VRP method was 38 percent higher than that of the conventional polishing. Figure 4.3 shows that the MRR of conventional polishing decreases along with the polishing time. On the other hand, the MRR of the VRP method hardly decreased for the polishing time of 10 minutes. This result indicates that the VRP method can sustain the polishing performance while the polishing time increases. The percent sustaining the material removal rate of the VRP method is higher than the conventional polishing as shown in Figure 4.4.

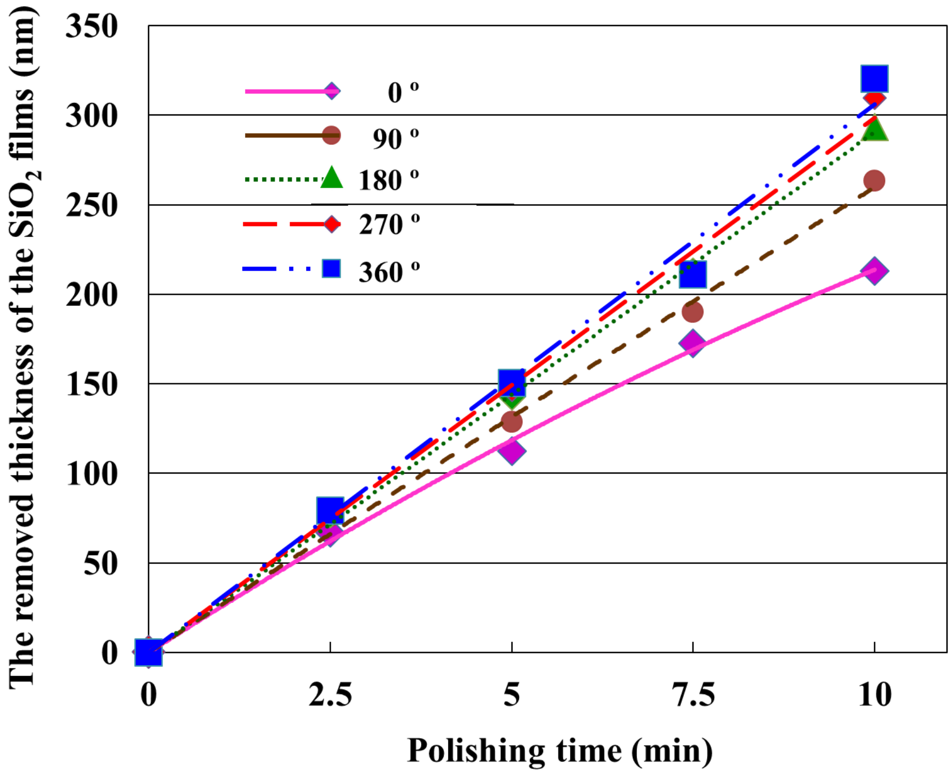


Figure 4.1: Dependence of the backward angles on the removed thickness of the SiO_2 films at various polishing times

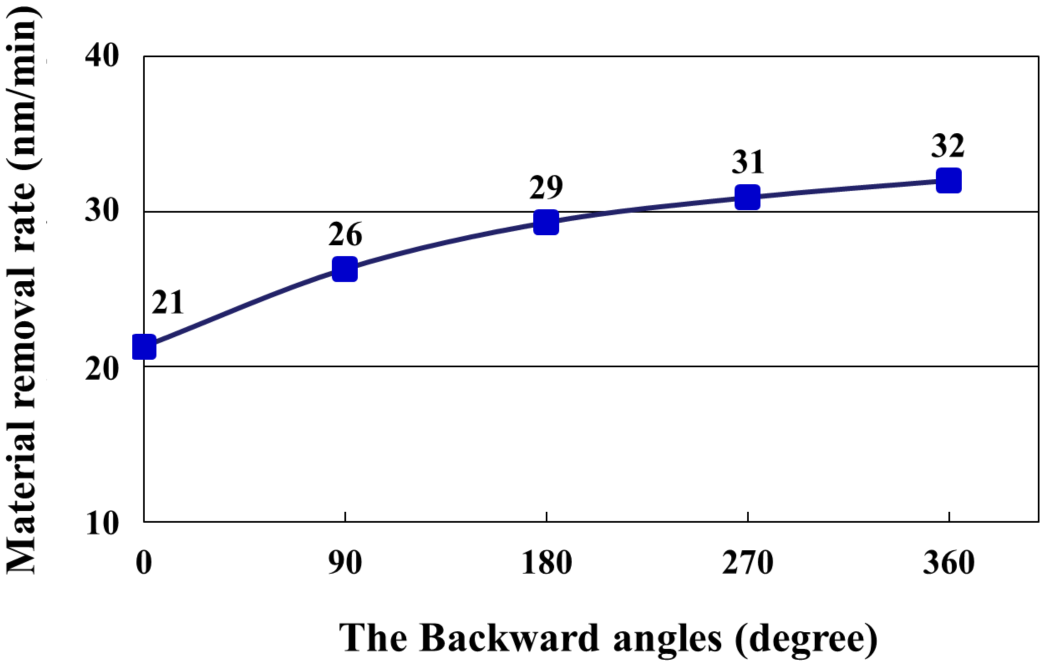


Figure 4.2: Dependence of the backward angles on the material removal rates at the 10 minutes polishing time

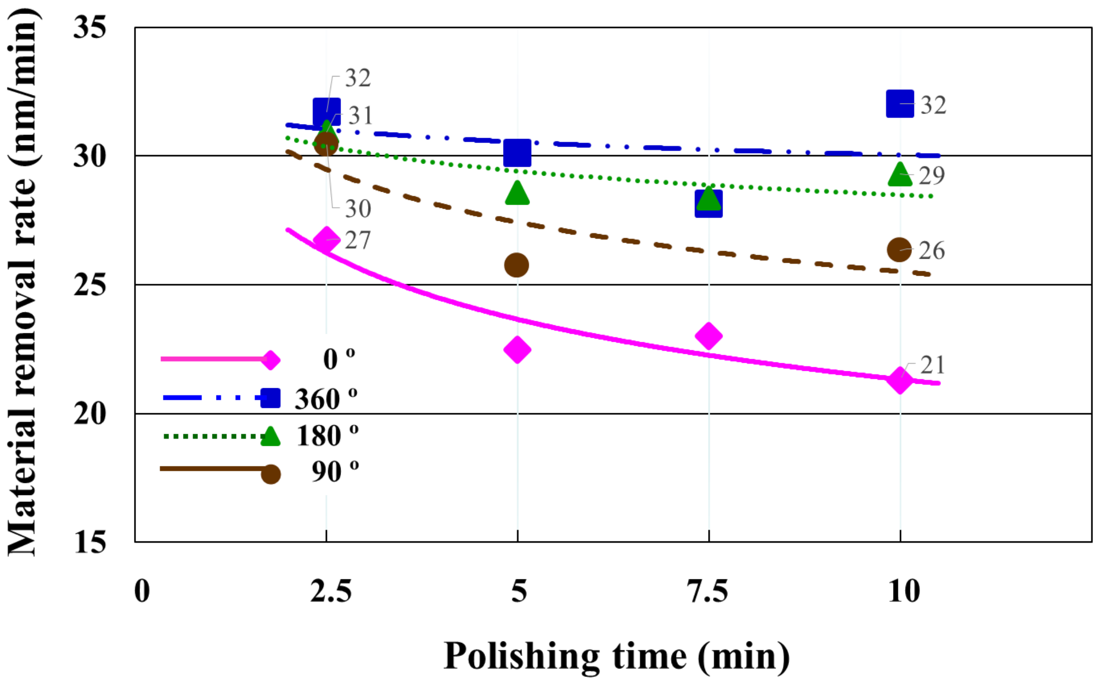


Figure 4.3: Dependence of material removal rate on polishing time at various rotational conditions

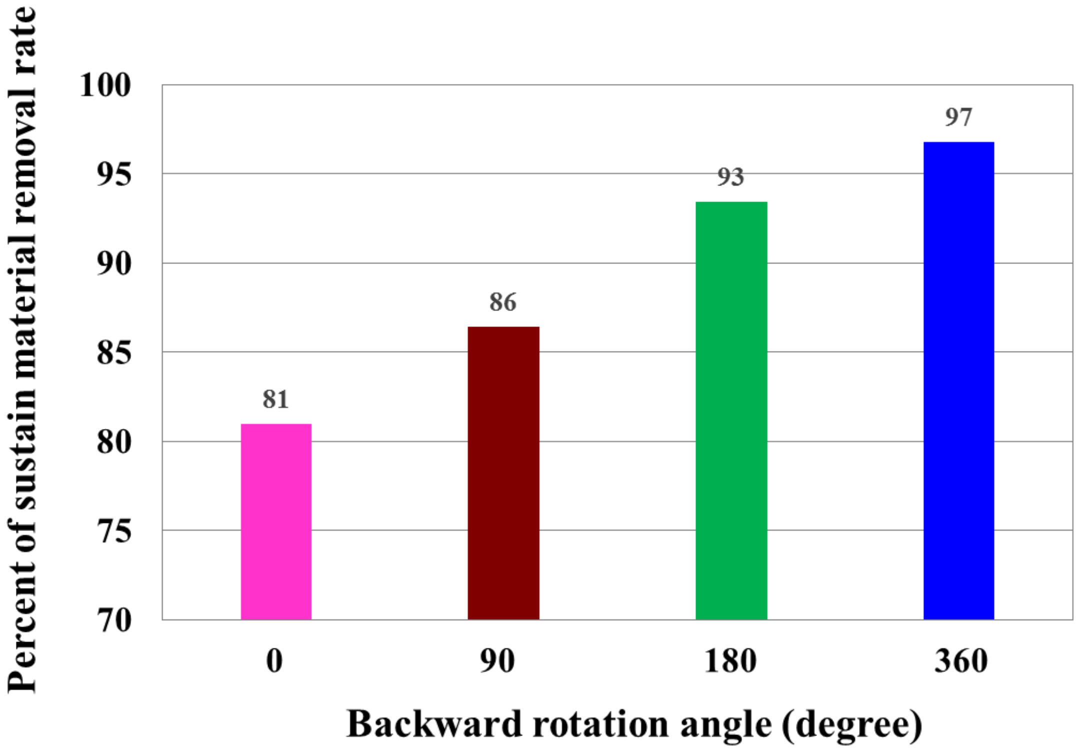


Figure 4.4: Percent sustaining material removal rate at various backward rotation angles

4.3 Summary

The experiment was designed to investigate the Variable Rotation Polishing method in order to improve polishing performance. The conclusions are as follows:

I. The material removal rate of the Variable Rotation Polishing was higher than that of the conventional polishing in all conditions. Particularly, the VRP method with 360 degrees backward rotation had the material removal rate 38 percent higher than that of the conventional polishing.

II. The material removal rate of the VRP method hardly decreased as the conventional polishing for the polishing time of 10 minutes. The VRP method was able to sustain the polishing performance despite an increased amount of polishing time. The percent sustaining the material removal rate of the VRP method was higher than that of the conventional polishing. In other words, the material removal rate was likely to be sustained by the VRP method.

III. The backward rotation angle caused an effect on the material removal rate. When the backward rotation angle was equal to the forward rotation angle, the material removal rate was higher.

Chapter 5

Mechanisms Analysis of the Variable Rotation Polishing Method

5.1 Introduction

The CMP process includes a number of parameters. The dominant parameters such as slurry flow distribution, slurry film thickness and asperity of polishing pad surface are evaluated through the cause and effect analysis (Fishbone diagram), in order to establish the sustention of the MRR during conventional polishing and the Variable Rotation Polishing as shown in Figure 5.1.

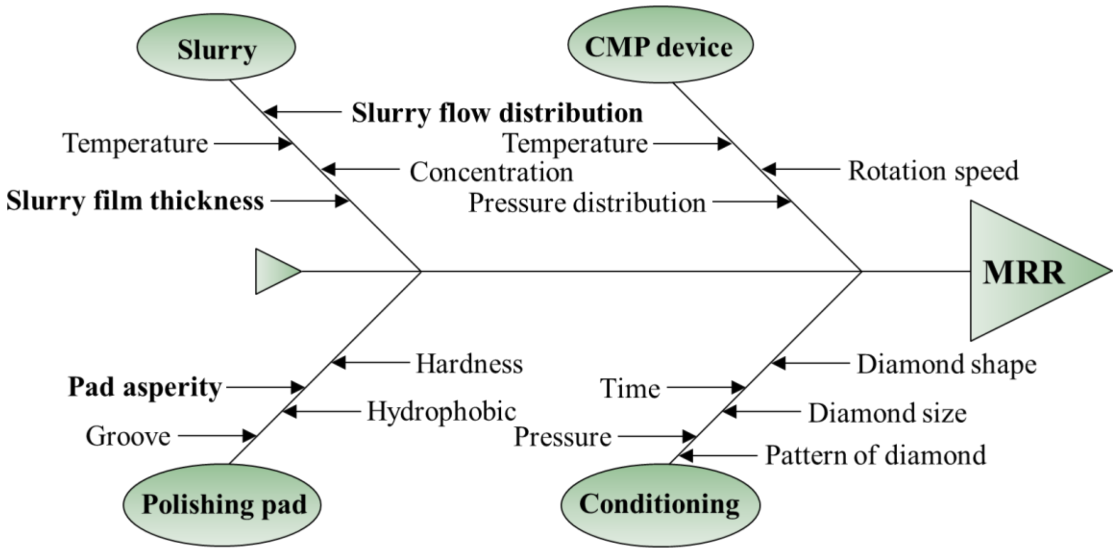


Figure 5.1: Cause and effect analysis (Fishbone diagram) of material removal rate of CMP process

5.2 Analysis around the wafer – pad contact area

The mechanism analyses were carried out as follows:

A) Slurry flow distribution observation (parameter I) as shown in Figure 5.2.

B) Slurry film thickness investigation (parameter II) as shown in Figure 5.3. This parameter likely relates to the shear force between the wafer and polishing pad.

C) Asperity on polishing pad surface (parameter III) as shown in Figure 5.4.

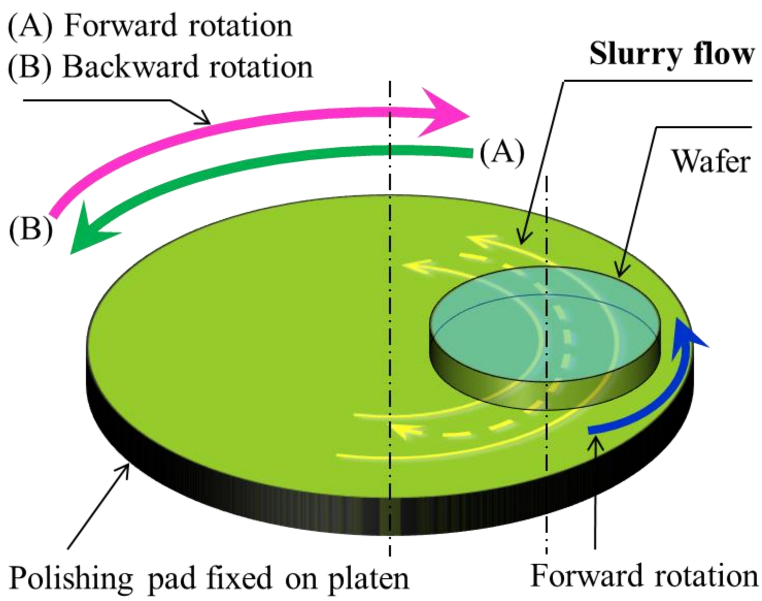


Figure 5.2: Slurry flow (parameter I) to sustain the material removal rate during CMP process

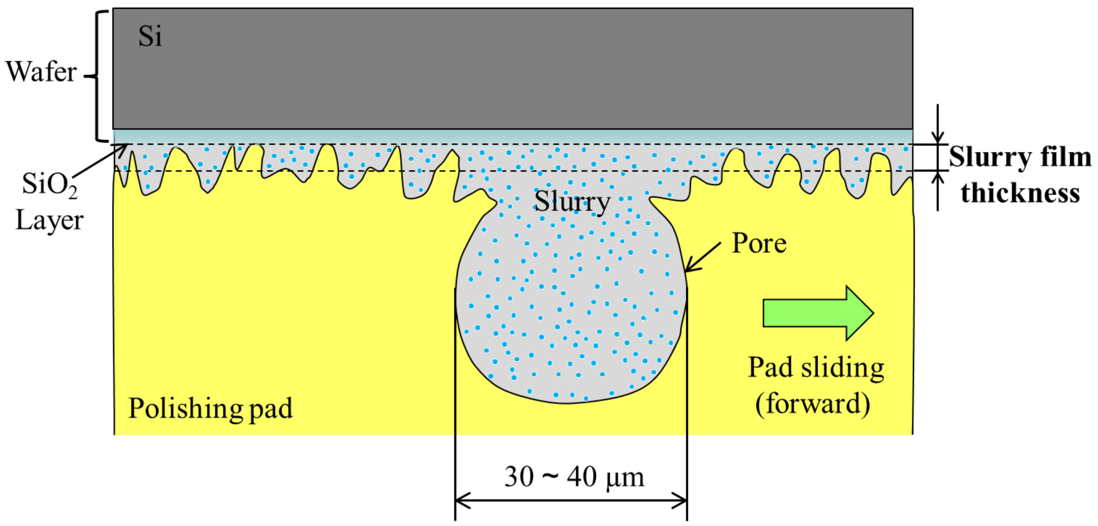
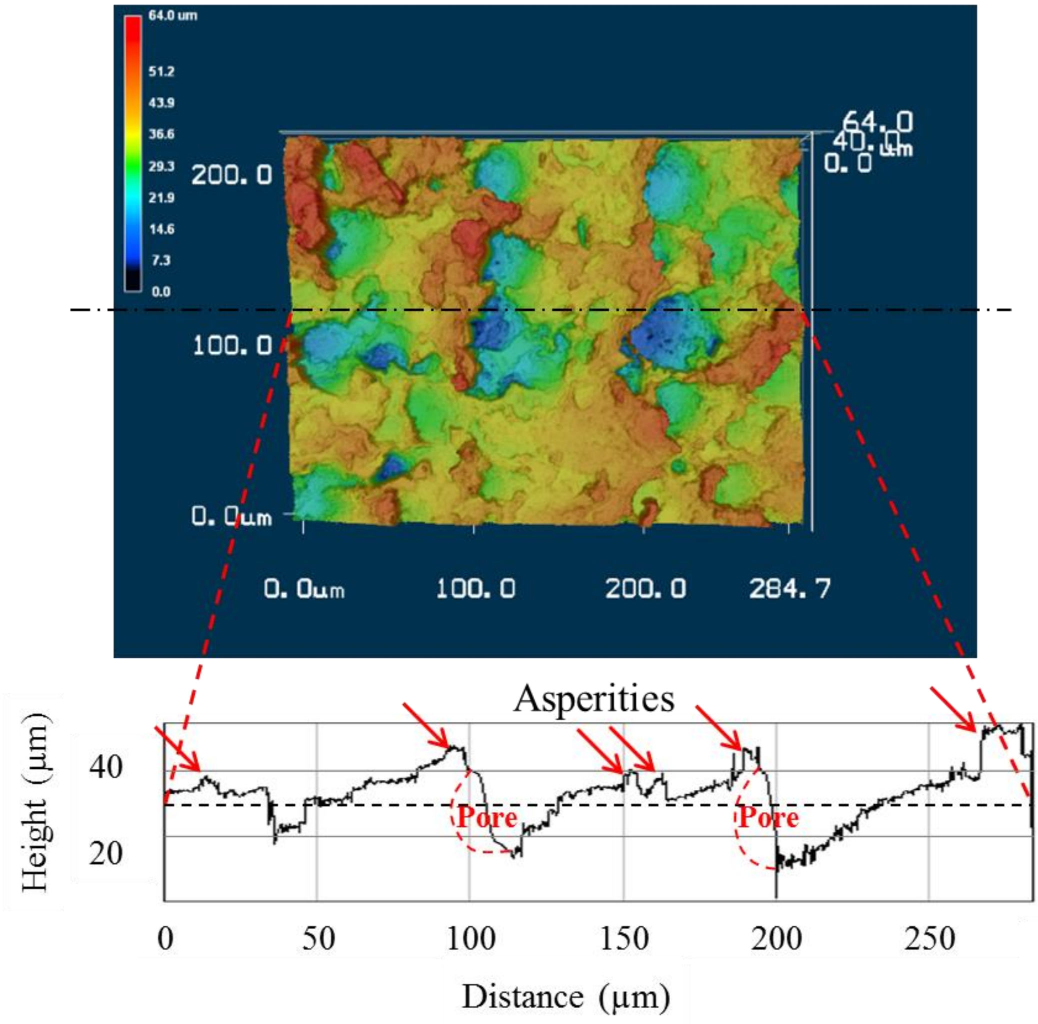


Figure 5.3: Slurry film thickness (parameter II) to sustain the material removal rate during CMP process

(a) Topography of the polishing pad surface by Confocal Laser Scanning Microscope



(b) Cross section profile of polishing pad after CMP process

Figure 5.4: Asperity on polishing pad surface (parameter III) to sustain the material removal rate during CMP process (a) Topography of the polishing pad surface by Confocal Laser Scanning Microscope, and (b) Profile of asperity after CMP process

5.2.1 Slurry flow observation

We observed the behaviour of the slurry between the wafer and polishing pad using the set of apparatus as illustrated in Figures 5.5 and 5.6 (appearance). The apparatus consists of the modified carrier which is held by the retainer ring. Figure 5.7 shows the modified carrier that allows observation of the slurry using a high speed camera because the bottom of the modified carrier is replaced with transparent quartz glass, which is in contact with the slurry and polishing pad. The slurry is replaced with the phosphor-luminous slurry, which is excited by UV light that will be captured by the high-speed camera [25, 30].

The intensity of luminescence phosphor was calculated using image processing software. The range of intensity or 8-bit grey value was set at the levels from 0 to 255. Figure 5.8 shows the top view of the slurry flow observation apparatus with a typical observed image from a high-speed camera consumed boundary, observation area (heart shape which is the only area used for analysis), reflection light from the quartz substrate and reflection light from the brass ring (both areas cannot be used for analysis). The intensity of phosphor luminous slurry’s grey value in conventional polishing was 88, evidently higher than that of the VRP method which was 63 as shown in Figure 5.9. This means that the slurry flow of the conventional polishing was spread more evenly than the VRP method. The results suggest that the slurry film thickness in the VRP method was qualitatively less than that of the conventional polishing.

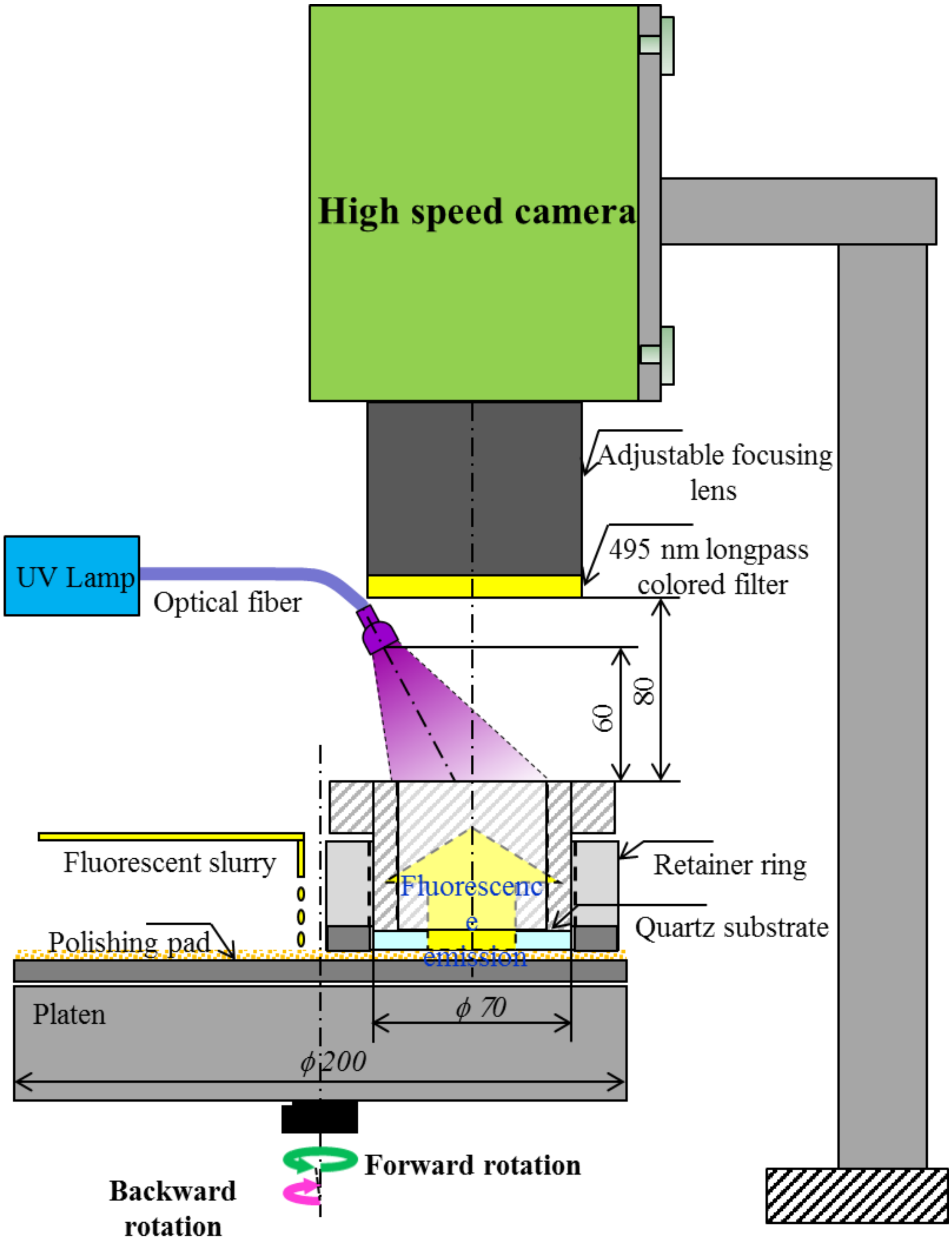


Figure 5.5: Schematic of experimental apparatus of slurry flow observation during CMP process

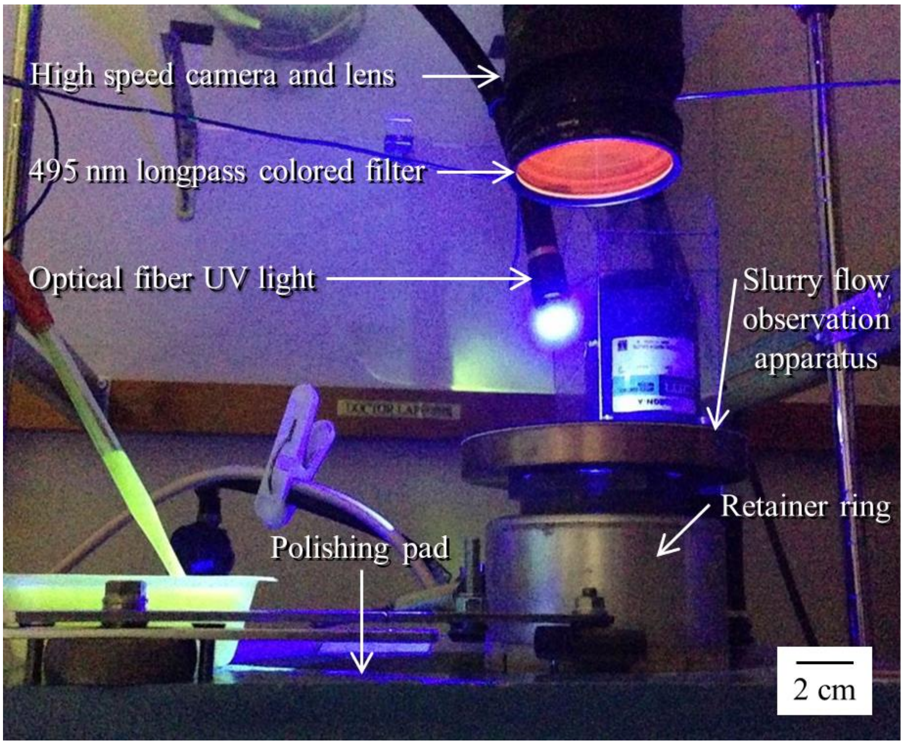
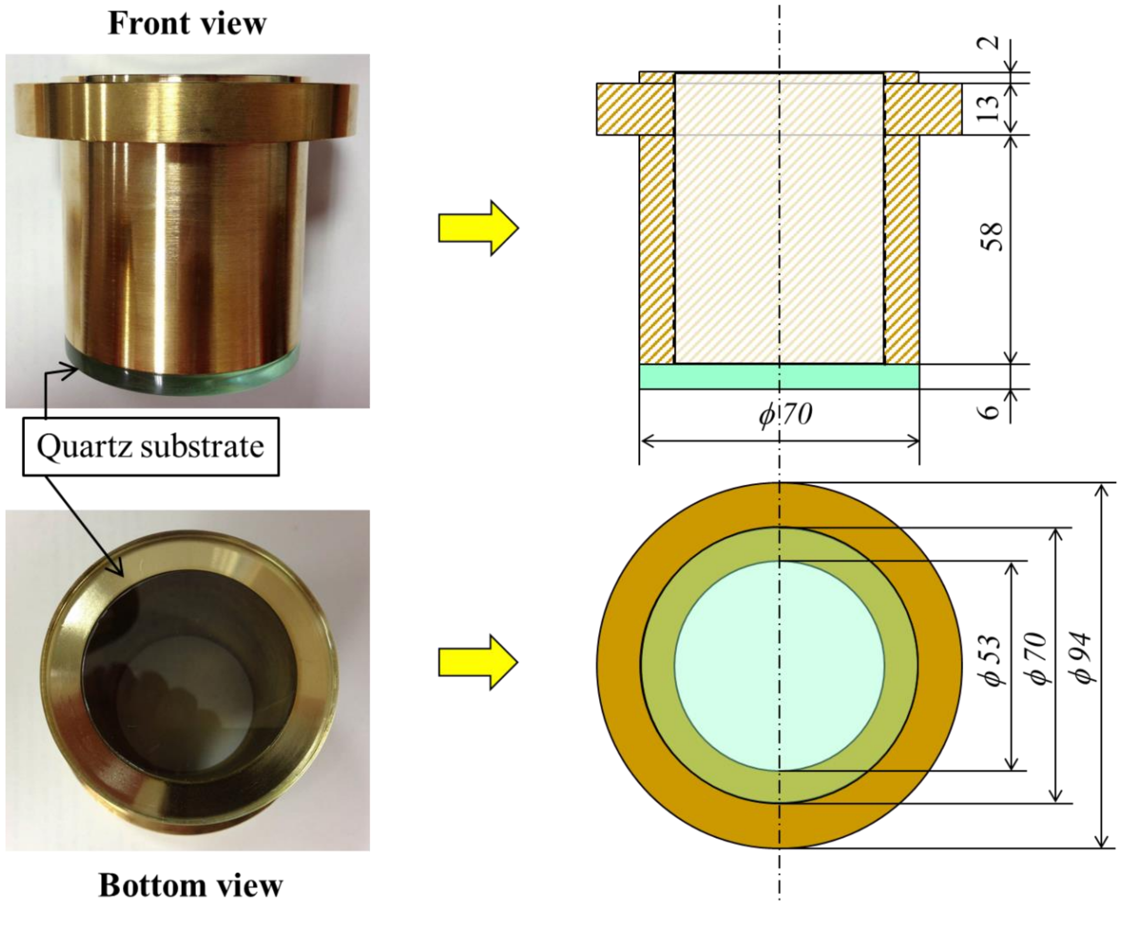


Figure 5.6: Appearance of the slurry flow observation apparatus



(a) Appearance of Modified carrier (b) Drawing of the modified carrier

Figure 5.7: Modified carrier for slurry flow observation

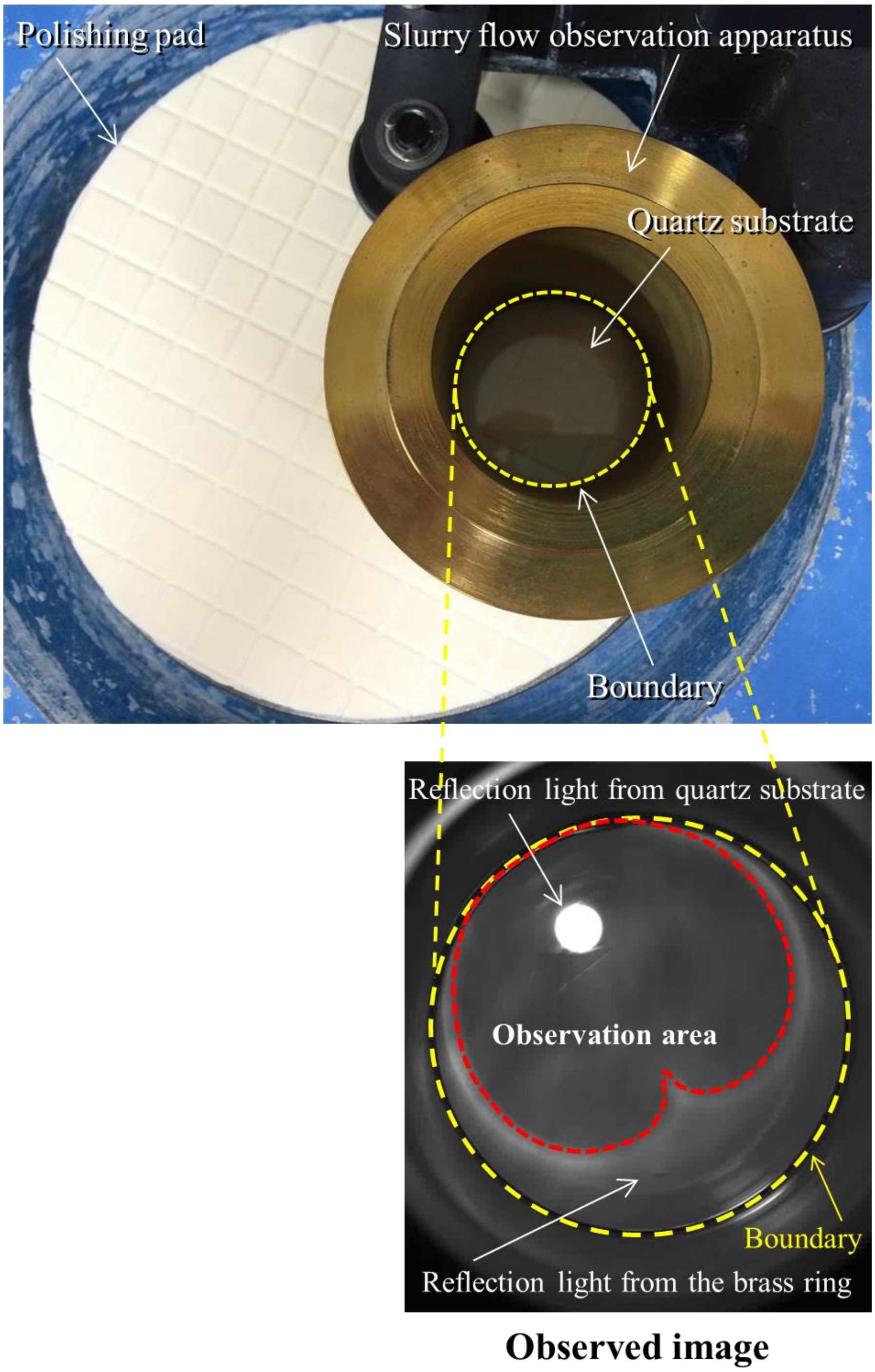
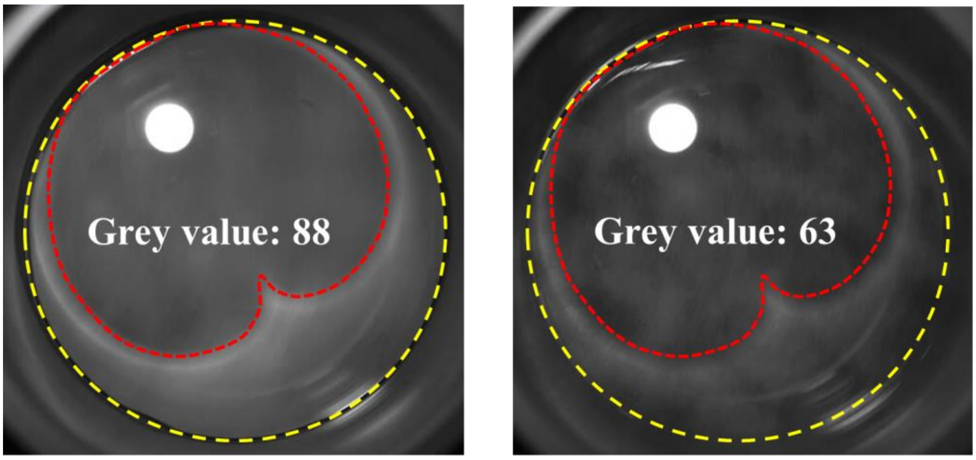
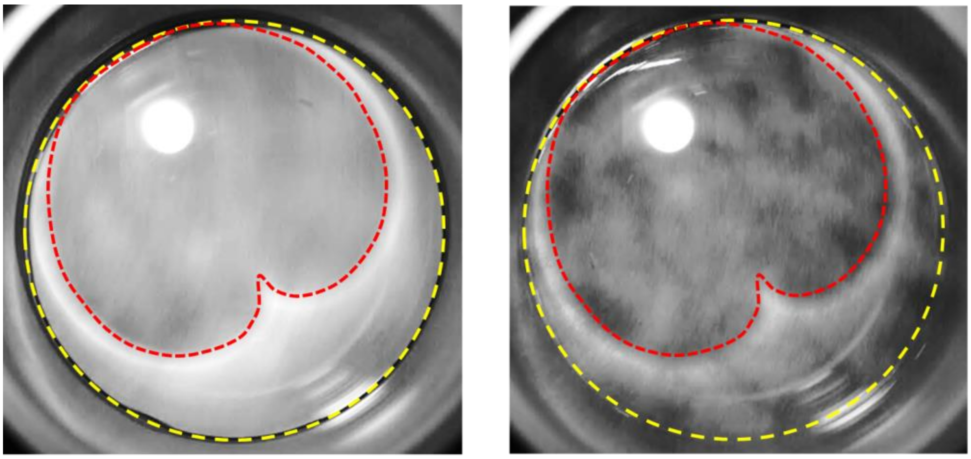


Figure 5.8: With a typical observed image from a high-speed camera (top view) with slurry flow observation apparatus



(a-1) Conventional polishing (b-1) VRP, forward 360º backward 360º

Unadjusted images captured by a high-speed camera



(a-2) Conventional polishing (b-2) VRP, forward 360º backward 360º

Post adjustment of brightness +40 % and contrast +40 %

Figure 5.9: Comparison of slurry flow distribution between polishing pad and wafer during conventional/VRP processes (a) Conventional polishing, and (b) VRP, forward 360º backward 360º

5.2.2 Slurry film thickness investigation

The variation of slurry film thickness during conventional/VRP CMP processes was evaluated from the vertical displacement values of the wafer carrier, which was set up at the top of the modified carrier. The displacement was obtained from the surface scanning laser confocal displacement meter; Keyence LT-9010M [31], as shown in the schematic diagram of measurement method in Figure 5.10. Figure 5.11 shows the schematic of the experimental setup, in which a silicon wafer was placed on the top of wafer carrier for detecting the reflected laser from the displacement meter [32]. Figure 5.12 shows the appearance of the experimental setup. Table 5.1 shows the specification of LT-9010M Model displacement meter.

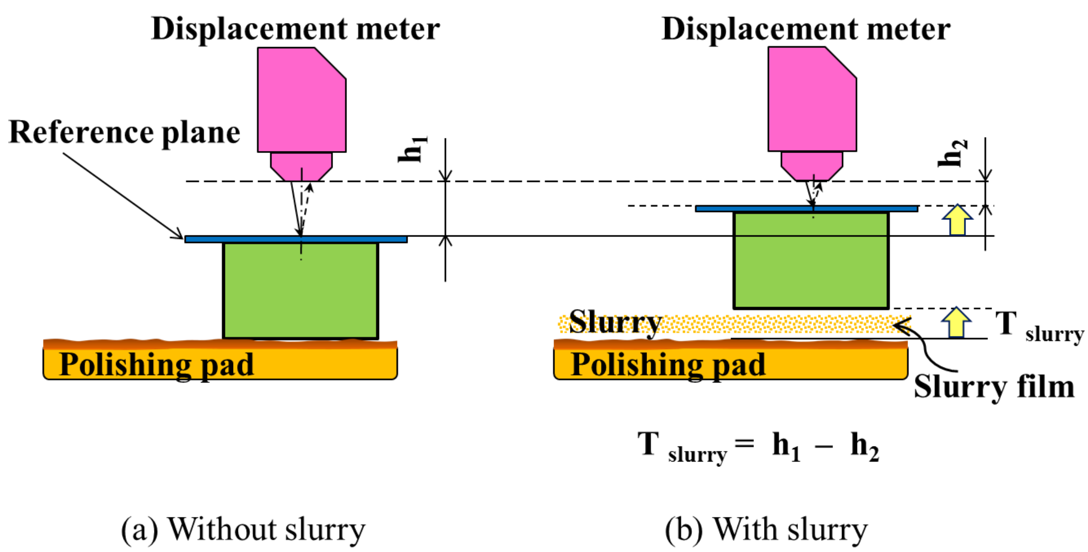


Figure 5.10: Measurement concept of varying slurry film thickness

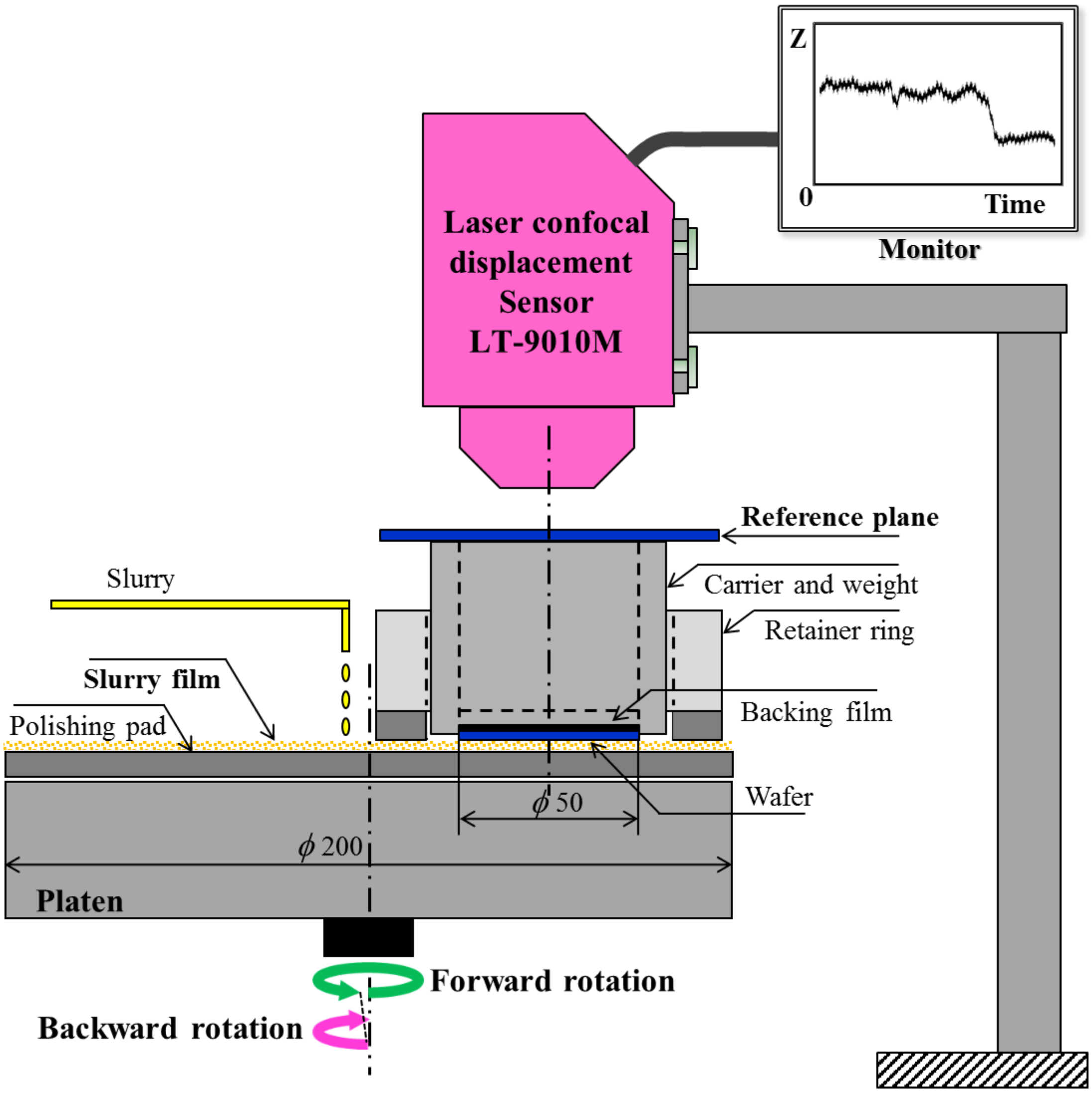


Figure 5.11: Experiment setup of wafer displacement measurement between the polishing pad and wafer during CMP process

From: http://www.keyence.com/products/measure/laser-confocal/lt-9000/models/lt-9010m/index.jsp.

Figure 5.12: Appearance of the experimental setup and the relation between the displacement meter and reference plane

Table 5.1: LT-9010M Model's specification

Model		LT-9010M
Measurement range	mm	±0.3
Reference distance	mm	6
Light source		
- Type		Laser diode
- Wavelength	nm	655
- Laser class		Class 1 (JIS C6802)
- Spot diameter	μm	Approx. ø2
Resolution	μm	0.01
Linearity		±0.5% of fit straight [*1]
Sampling cycle	ms	0.640 to 356 (14 steps)
Microscope function		
- Field of view	mm^2	1.3 × 1.05
- Infrared LED light source		wavelength: 870 nm
Temperature characteristics (20 to 30°C)		±0.5% of fit straight
Weight	g	400 (approx.)

[*1] The value when the measurement target is a mirrored surface object measured in displacement mode, scan width/interval 120 μm/ 2 μm, and 8-times average.

Figure 5.13 shows a slurry film thickness measurement flowchart. The wafer displacement values (raw data) in the conventional polishing and VRP method are shown in Figure 5.14. The wafer displacement values in the case of VRP method were estimated to be 8 µm on average. It was found that the values of VRP method were thinner than those of the conventional polishing, as shown in Figure 5.15. Based on the values obtained from the slurry flow distribution and wafer displacement measurements, the thickness of the slurry between the polishing pad and wafer during the VRP method was 1 μm thinner than that of the conventional polishing as shown in Figure 5.16. There has been reported that the shear force and MRR are investigated to be inversely proportional to the slurry film thickness [22]; therefore, a thinner slurry film in the VRP method is likely to cause a larger shear force and MRR [23].

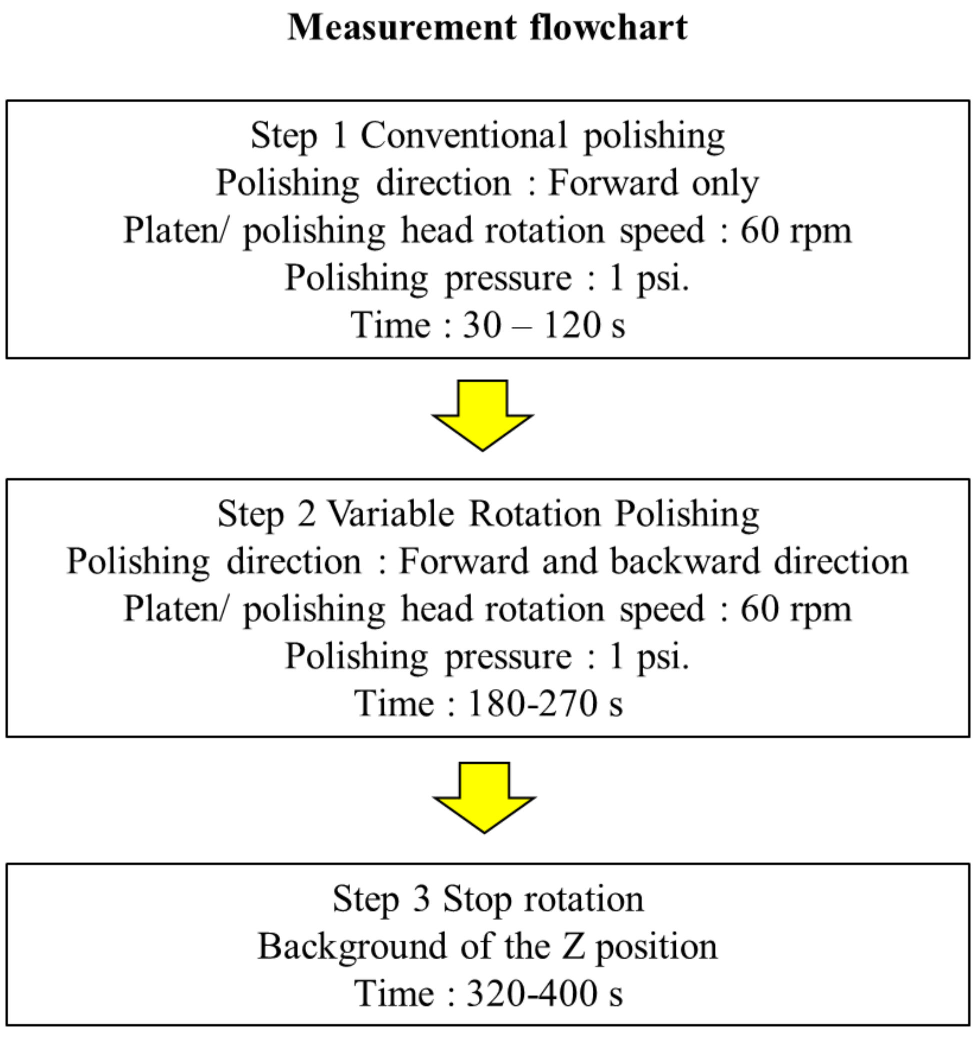


Figure 5.13: Measurement flowchart of the change of slurry film thickness

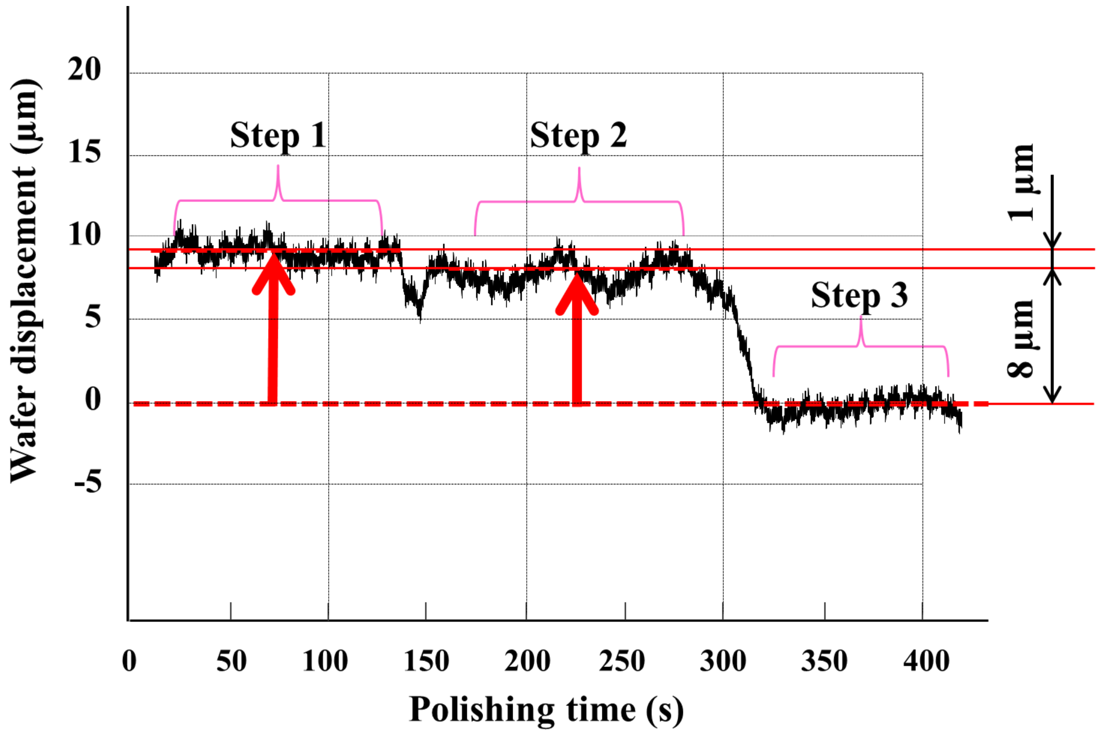


Figure 5.14: Wafer displacement values between the polishing pad and SiO_2 wafer during CMP process

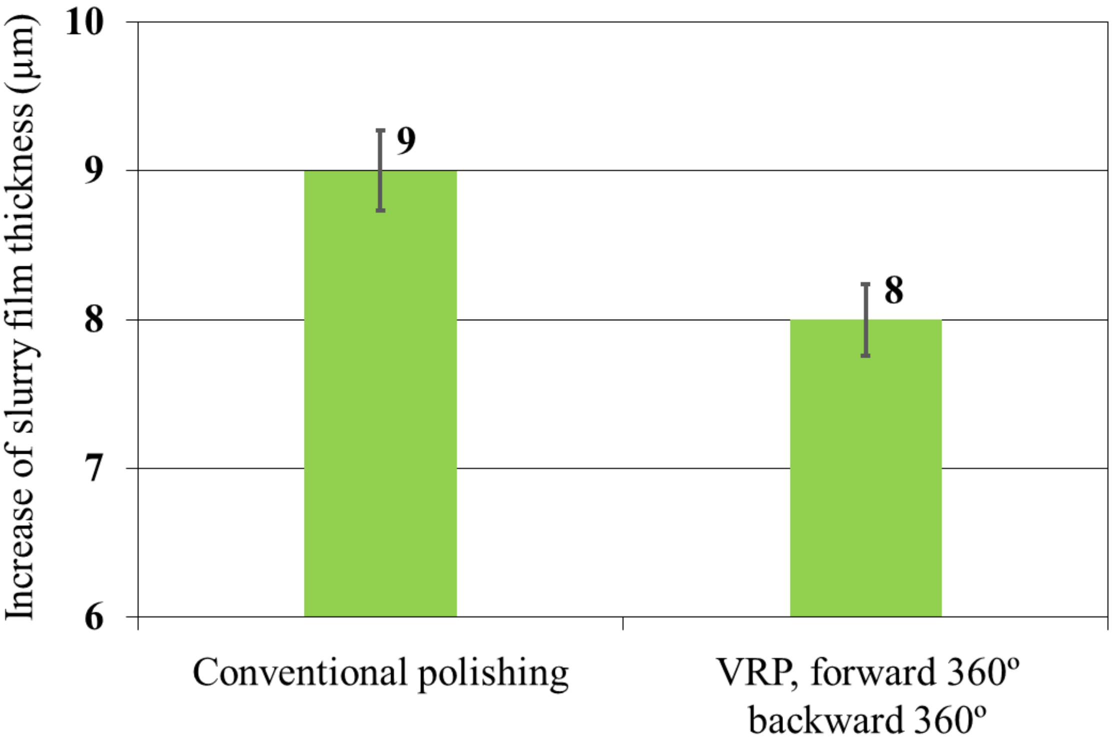
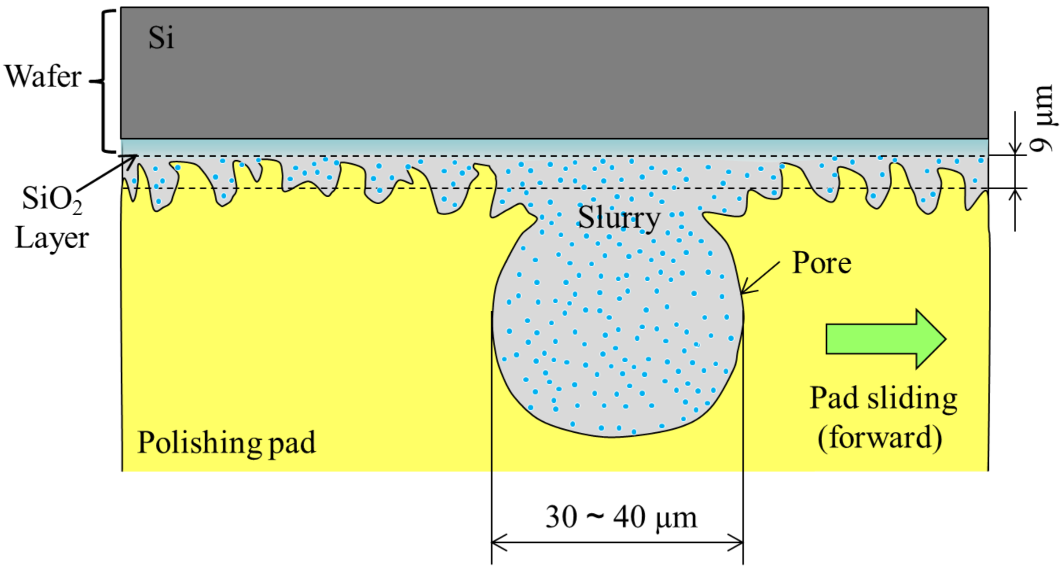
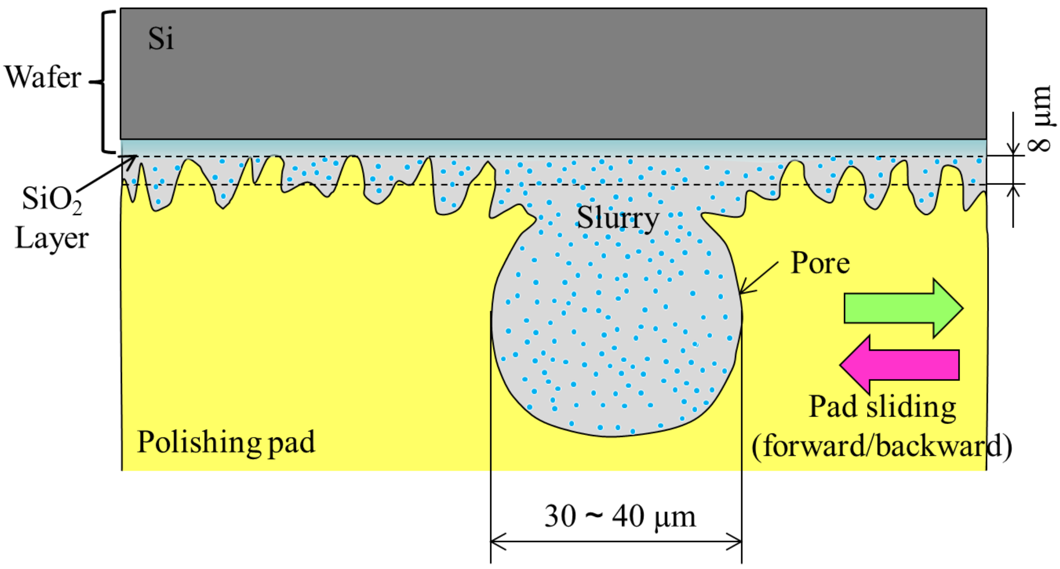


Figure 5.15: Decrease of slurry film thickness in the VRP method between polishing pad and SiO_2 wafer during CMP process



(a) In the case of conventional polishing



(b) VRP, forward 360º backward 360º

Figure 5.16: Difference of slurry film thickness displacement during the conventional/ VRP CMP processes

5.2.3 Asperity on polishing pad surface

In order to determine the underlying factor of VRP method that increases the polishing efficiency, the asperity on a polishing pad surface after CMP process was observed using a confocal laser scanning microscope. Two points on a polishing pad were selected to be measured before/after polishing, as shown in Figure 5.17. The two points on a polishing pad, which were dried after polishing, were measured with a confocal laser scanning microscope; Keyence VK-9710. Figure 5.18 shows typical asperities and pores (3D) at the polishing pad measurement point I in the case of conventional polishing and VRP, forward 360º backward 360º. Figure 5.19 shows typical asperities and pores (3D) at the polishing pad measurement point II in the case of conventional polishing and VRP, forward 360º backward 360º. Figure 5.20 shows typical asperities and pores on polishing pad after CMP process at the measurement point I. Figure 5.21 shows typical asperities and pores on polishing pad after CMP process at the polishing pad measurement point II. As a result, the profiles of asperity in case of conventional polishing were bent and covered pore in contrast to the VRP, forward 360º backward 360º where the profiles were not bent and maintained to stand.

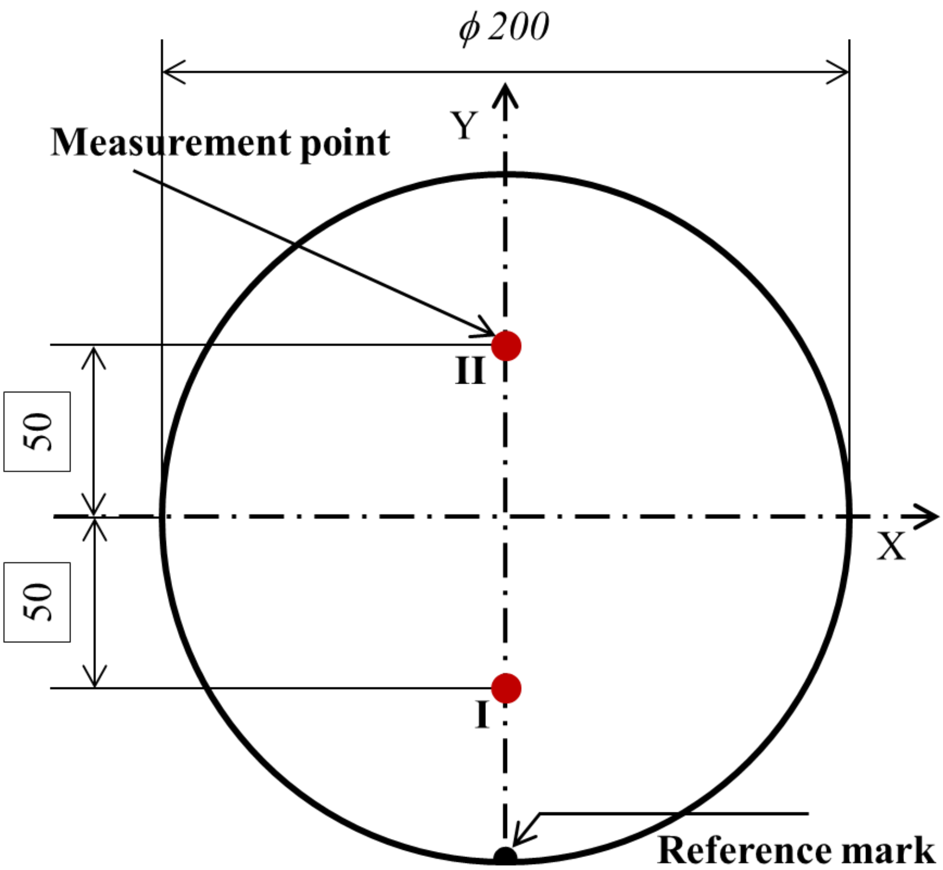
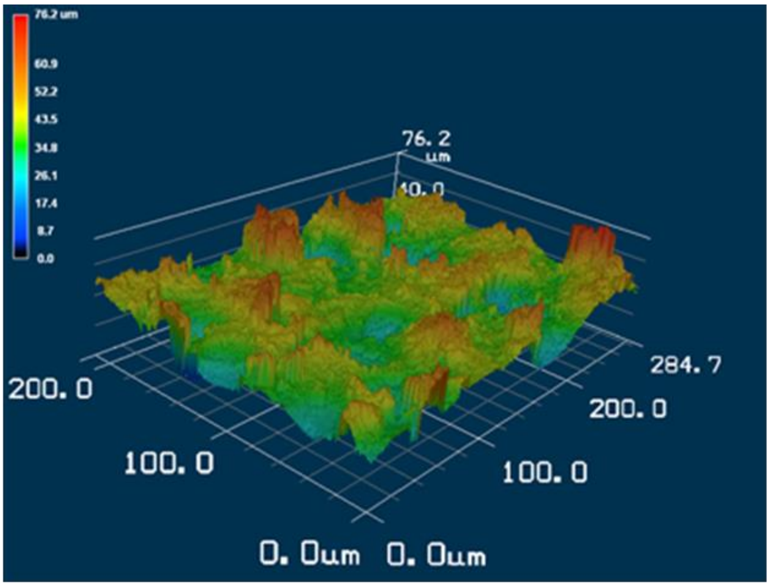
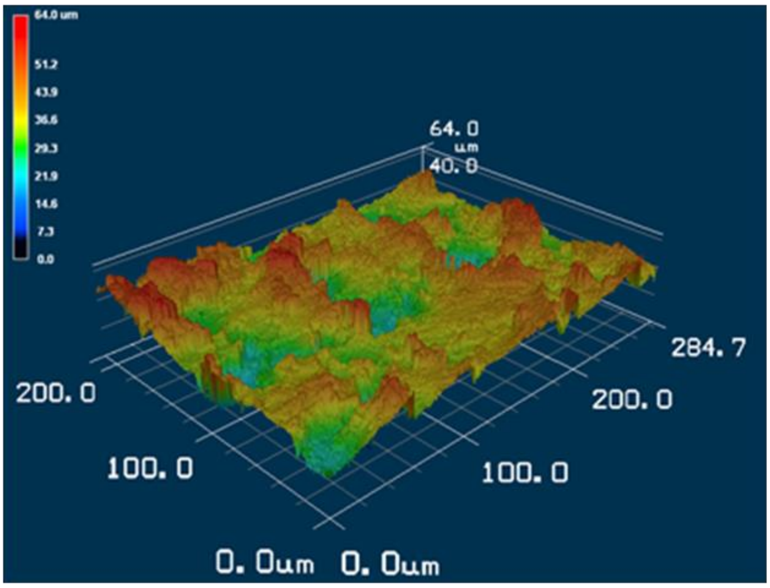


Figure 5.17: 2 points of measurement on polishing pad

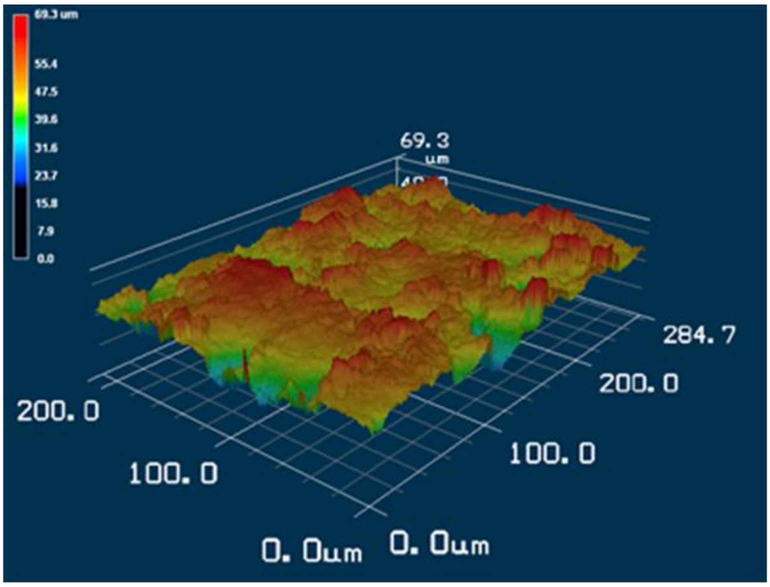


(a-1) Conventional polishing point I

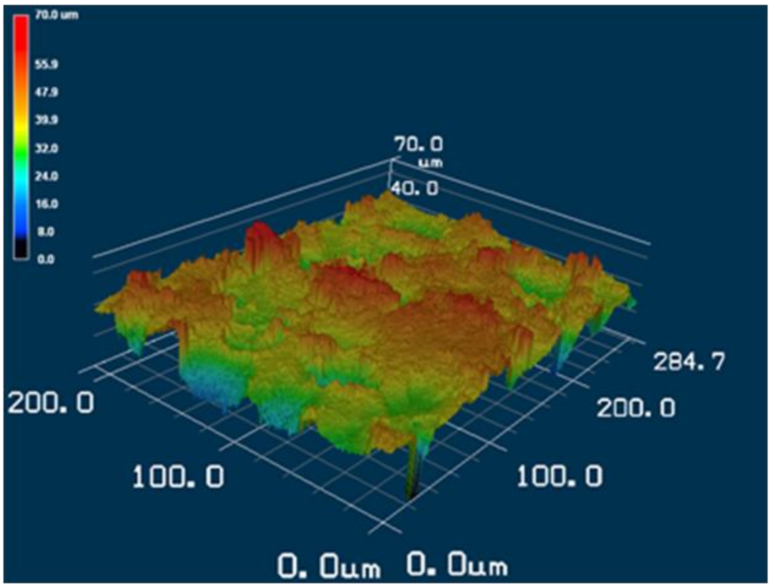


(b-1) VRP, forward 360° backward 360° point I

Figure 5.18: Typical asperities and pores (3D) on a polishing pad after CMP process

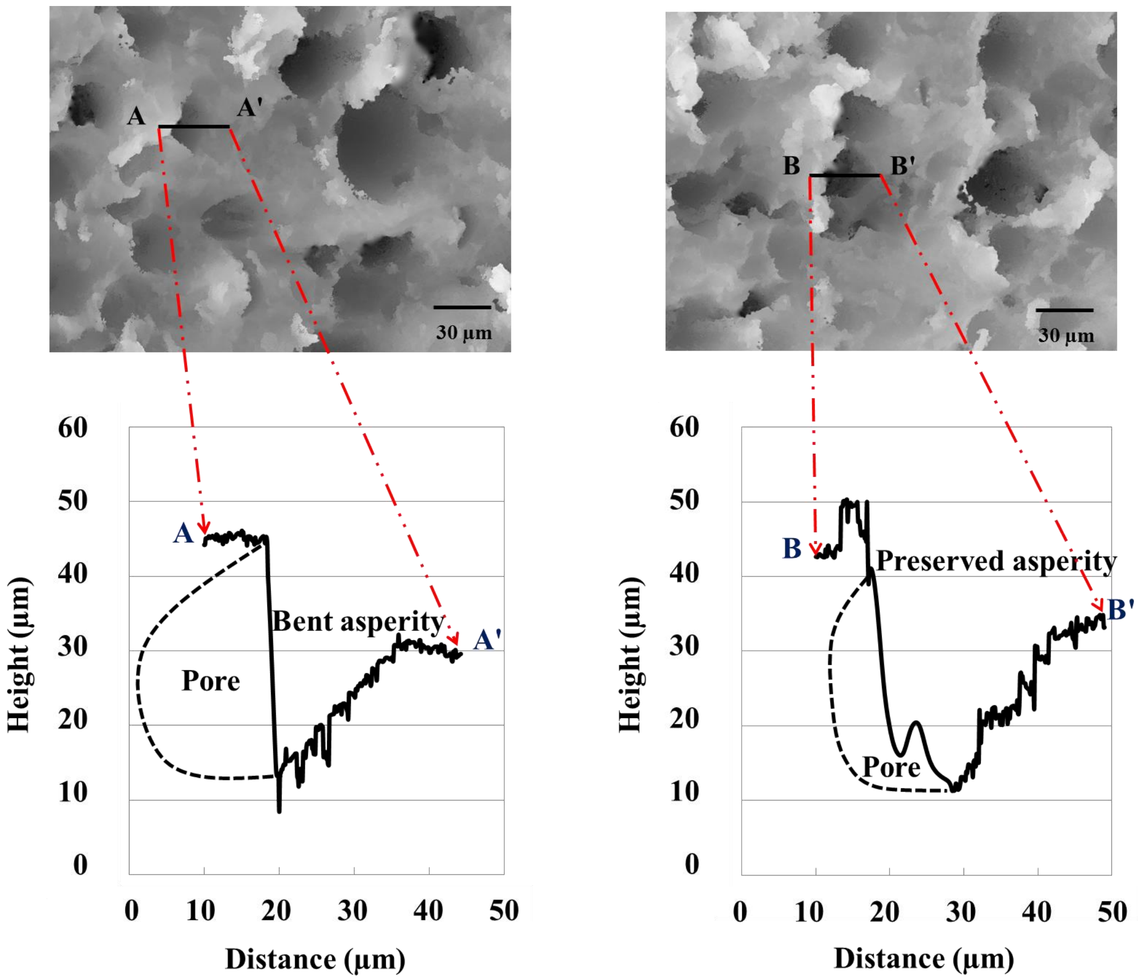


(a-2) Conventional polishing point II



(b-2) VRP, forward 360° backward 360° point II

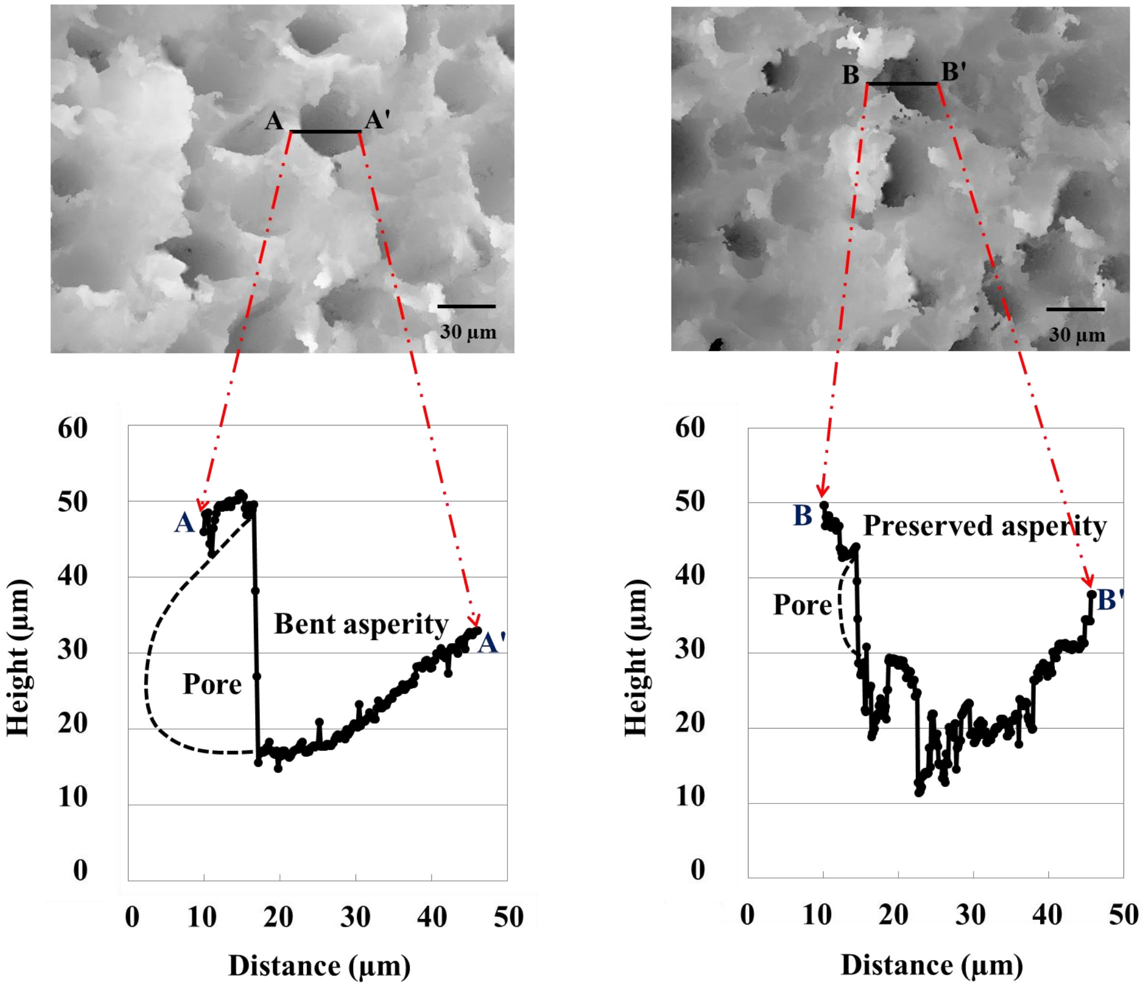
Figure 5.19: Typical asperities and pores (3D) on a polishing pad after CMP process



(a-1) Conventional polishing point I

(b-1) VRP, forward 360º backward 360º point I

Figure 5.20: Typical asperities and pores on polishing pad after CMP process



(a-2) Conventional polishing point II

(b-2) VRP, forward 360º backward 360º point II

Figure 5.21: Typical asperities and pores on polishing pad after CMP process

5.3 Modeling of asperities on polishing pad surface during CMP process

Based on cause and effect analysis (Fishbone chart), the 3 underlying parameters of CMP process that affect the polishing efficiency were determined. The slurry flow distribution, slurry film thickness, and polishing pad asperities, were investigated. For the experimental results, a model is constructed in order to explain the material removal mechanism in the contact area during CMP process.

The conventional rotation polishing is the method that the asperity receives one directional load, leaves the asperity bending in one direction, and conducts the slurry flow in one direction. Note that several pores on the polishing pad are covered by those angled asperities.

The method in this study appears to preserve the asperity since the bidirectional movement maintains the asperity upright across the polishing pad. The behaviour of polishing pad asperity in the conventional CMP process is separated into 3 stages as follows:

$t = 0$: The entire asperities on polishing pad surface stand upright (after conditioning).

$t = t_F$: After forward rotation started, asperities on polishing pad surface is slightly bending to one side.

$t \gg t_F$: Asperities are bent in one direction by forward rotation.

In the conventional polishing, the asperities on the polishing pad surface are bent in one direction for all the time. The result starting from t = 0 to the asperity condition is bent one side and the CMP process finishes is shown in Figure 5.22.

The behaviour of polishing pad asperities in the VRP method would be separated into 3 stages as follows:

$t = 0$: The entire asperities of polishing pad surface stand upright (after conditioning).

$t = t_F$: Asperities of polishing pad surface is slightly bending to one side by forward rotation

$t = t_B$: Asperities of polishing pad surface are slightly bent back to the other side by backward rotation.

In the Variable Rotation Polishing method, the asperities would be reserved because the asperities are not bent down in only one direction but the bent-down asperities are slightly bent up again during backward rotation as shown in Figure 5.23. This behaviour would causes the asperities to stand upright for a long period of time.

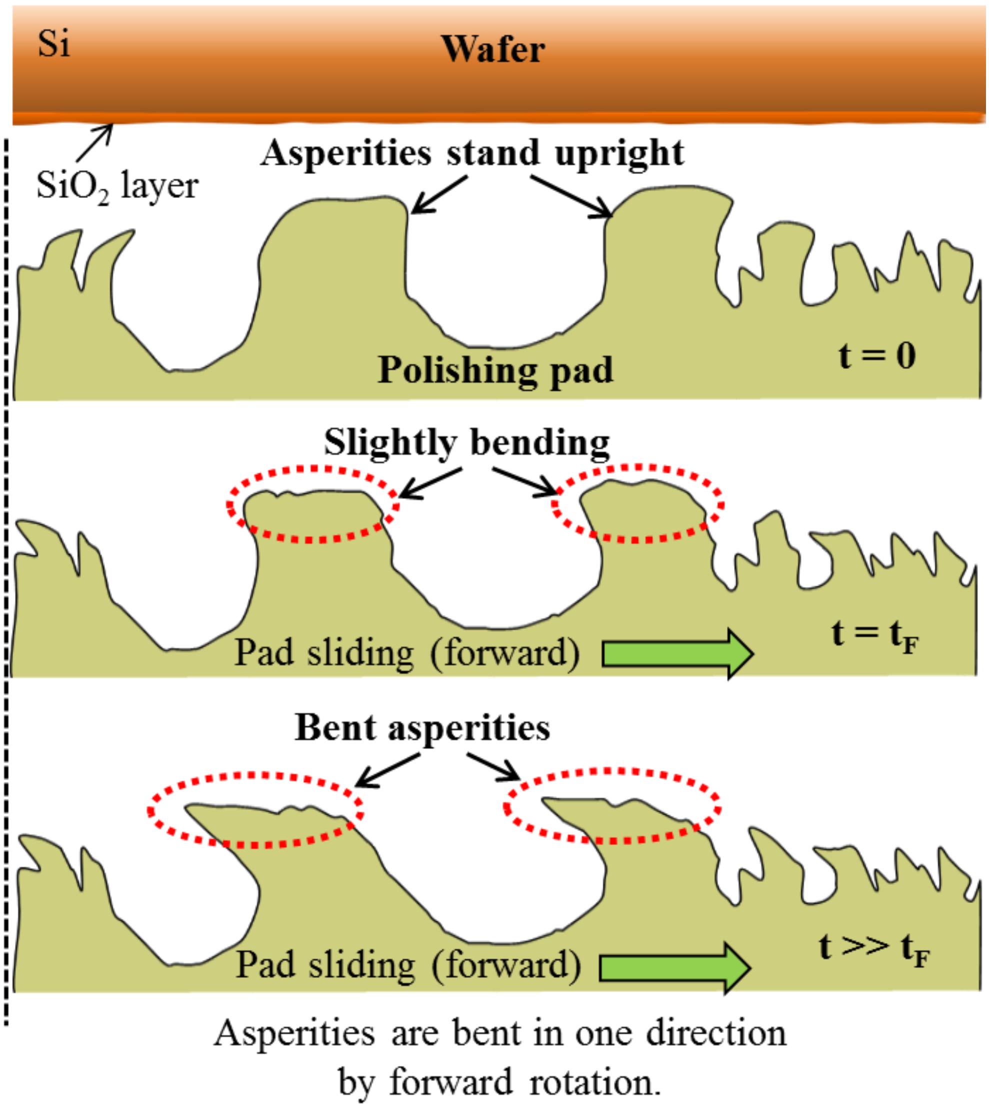


Figure 5.22: Behavior of asperities on polishing pad surface during CMP process in the case of conventional polishing

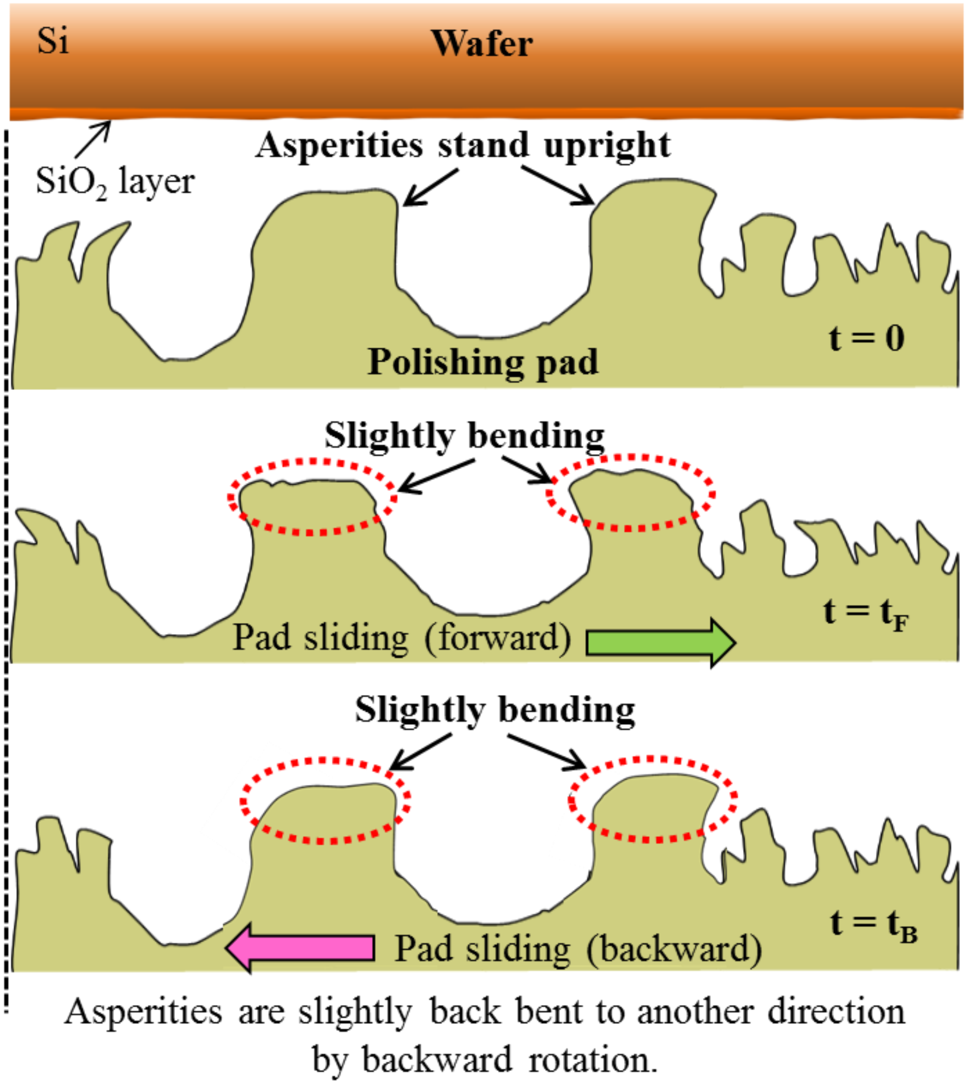


Figure 5.23: Behavior of asperities on polishing pad surface during CMP process in the case of VRP method

5.4 Discussion

The slurry flow distribution in the Variable Rotation Polishing method became comparatively uneven due to its bending in both directions, even though the MRR was higher than that of the conventional polishing.

The thickness of the slurry film in the case of Variable Rotation Polishing was 1 μm on average thinner than that of the conventional polishing. This implies that the VRP method would perform a larger shear force in CMP to enhance the MRR.

The typical asperities and pores (3D) on polishing pad surfaces after the CMP process were measured. The results were compared between the conventional polishing method and the VRP method with the rotational angle forward 360 backward 360 at points I and II. It was concluded that in the case of conventional polishing, the asperity on polishing pad surface was bent in one direction all the time. Consequently, the asperity height became lower and subsequently decreased the MRR. On the other hand, in the Variable Rotation Polishing method, the asperity of the polishing pad surface was stood upright by backward rotation, which resulted in a higher MRR. Finally, the behavior of polishing pad asperity during CMP was modelled to explain the reason of the higher MRR in the VRP method.

5.5 Summary

The pad conditioning treatment generally acts to define and maintain the structure of the asperities on polishing pad surface and affects the material removal rate and material removal stability. Without conditioning treatment of the pad surface during polishing, the material removal rate rapidly decreased corresponding to the polishing time. Because the asperities on polishing pad surface becomes smoother (bent to one direction), i.e. the asperity height becomes lower [33-36]. In case of VRP method, the asperities on polishing pad surface is kept standing upright by backward rotation. Therefore, the conditioning treatment would be less necessary to obtain the required steady pad asperity height to sustain the material removal rate. As mentioned above, the asperities height on the polishing pad surface is a very important parameter to perform an efficient CMP.

Chapter 6

Polishing Pad Analysis by 3D Topography Observation

6.1 Introduction

From chapter 5, the pad conditioning treatment acts to define and maintain the structure of the asperities on polishing pad surface. The asperities on polishing pad surface have strong correlation with the material removal rate in the CMP process. It is known that the pad conditioning treatment has a strong effect on the material removal rate and the material removal rate stability [33, 34]. In general, the conditioning treatment is necessary for conventional polishing and MRRs decrease along with the polishing time as shown in Figure 6.1. In the case of the VRP method, the asperities on polishing pad surface are influenced by backward rotation of the platen. Therefore, the conditioning treatment is unnecessary to obtain the required steady state condition of the pad surface [27, 35-39]. Furthermore, the material removal rate and the asperity height are sustained significantly according to the polishing time without the conditioning treatment. In this chapter, the 3D topography of a polishing pad surface was observed in order to determine the dominant parameter contributing to high MRRs in the VRP method. The behaviour of asperity should account for the material removal rate and the asperity height being sustained significantly according to the polishing time without the conditioning treatment.

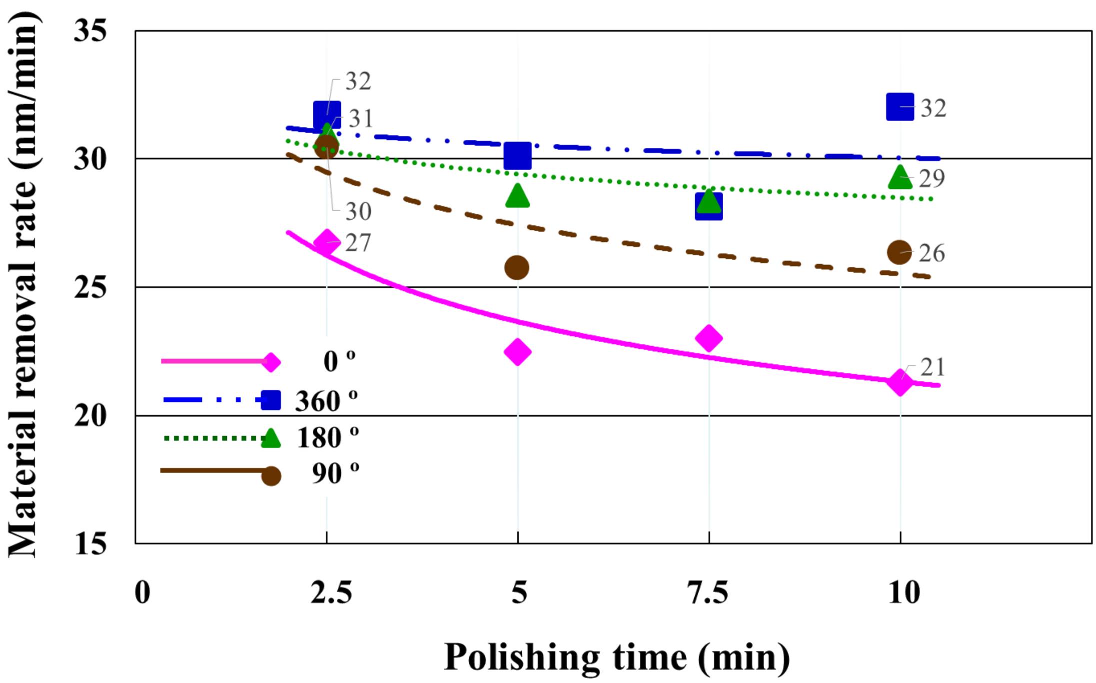


Figure 6.1: MRR decreases as polishing time increases.

6.2 Polishing pad analysis

6.2.1 3D topography observation

3D topography observation was used for polishing pad analysis and measuring the roughness of asperity on polishing pad surface. Figure 6.2 shows topography height of asperities on polishing pad surface after conditioning treatment, after 10 minutes polishing in the case of conventional polishing, and the VRP method. The topography of the height of asperities on polishing pad surface after a conditioning treatment is shown in Figure 6.3. The asperities on polishing pad surface after 10 minutes polishing in the case of conventional polishing at point I are shown in Figure 6.4 and those at point II in Figure 6.6. The asperities on polishing pad surface after 10 minutes polishing in the case of VRP, forward 360^{o} backward 360^{o} at point I are shown in Figure 6.5 and point II in Figure 6.7.

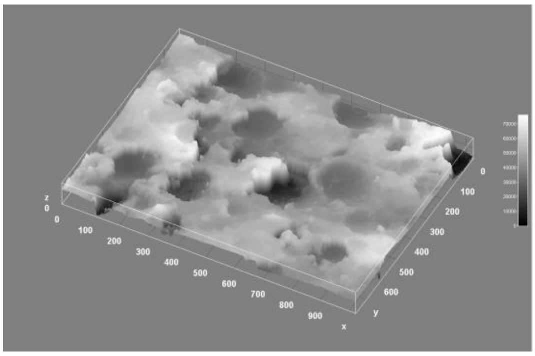
In Figures 6.2 - 6.7, a comparison is not clear. As a result, an analysis is made by cutting out the asperities below 20 μm from the top while the top of 20 μm of the asperity on polishing pad surface remains. Figure 6.8 shows topography the top of 20 μm of height of asperities on polishing pad surface after conditioning treatment, after 10 minutes polishing in the case of conventional polishing, and in the case of the VRP method. The roughness of asperity on polishing pad surface is analysed based on 3 criteria as follows:

Criterion 1 20 µm of asperities height on the top of polishing pad surface after conditioning treatment is shown in Figure 6.9.

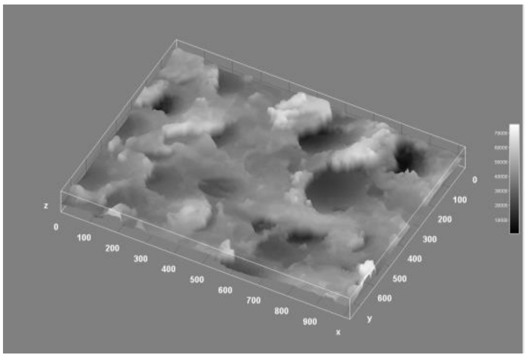
Criterion 2 20 µm of asperities height on the top of polishing pad surface after 10 minutes polishing in the case of conventional polishing at point I is shown in Figure 6.10 and those at point II in Figure 6.12.

Criterion 3 20 µm of asperities height on the top of polishing pad surface after 10 minutes polishing in the case of VRP, forward 360º backward 360º at point I is shown in Figure 6.11 and those at point II in Figure 6.13.

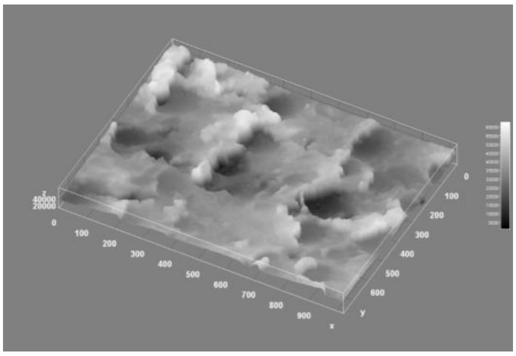
Figures 6.8 – 6.13 compare the asperities height at 20 µm on the top of polishing pad surface between conventional polishing and the Variable Rotation Polishing method. The asperity height in the VRP method after a conditioning treatment has almost the same and still has asperity at 20 µm from the top. On the other hand, there is less asperity below 20 µm from the top in the case of conventional polishing.



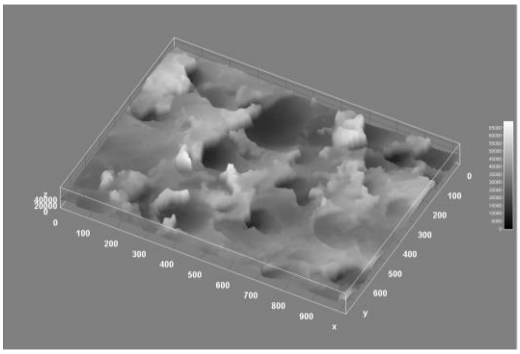
(a) After conditioning treatment



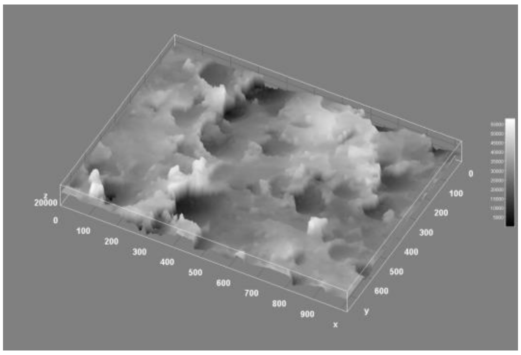
(b-1) Conventional polishing point I



(c-1) VRP, forward 360º backward 360º point I



(b-2) Conventional polishing point II



(c-2) VRP, forward 360º backward 360º point II

Figure 6.2: Asperities on polishing pad surface: (a) after conditioning treatment, and after 10 minutes polishing (b) in the case of conventional polishing at point I, II (c) in the case of VRP, forward 360º backward 360º at point I, II

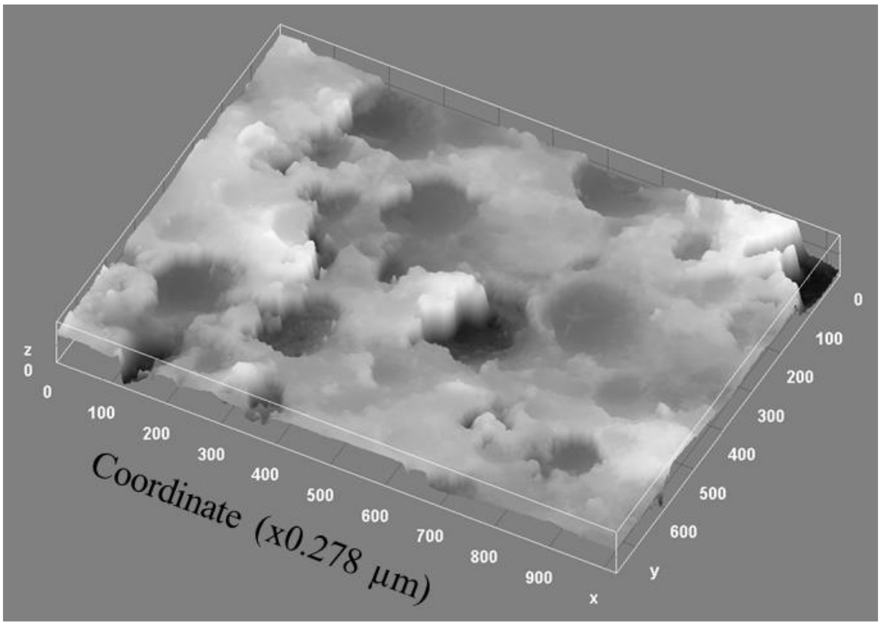


Figure 6.3: Asperities on polishing pad surface after a conditioning treatment

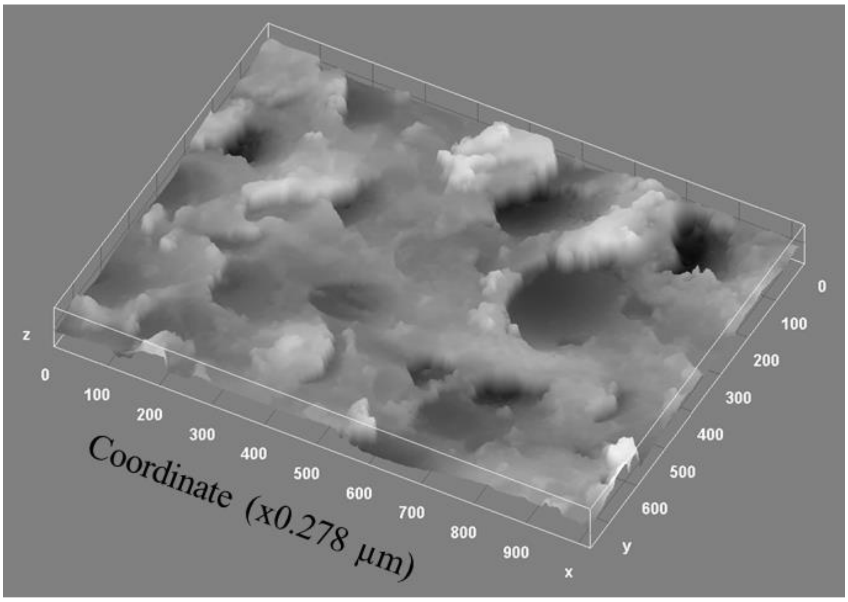


Figure 6.4: Asperities on polishing pad surface after 10 minutes polishing in the case of conventional polishing at point I

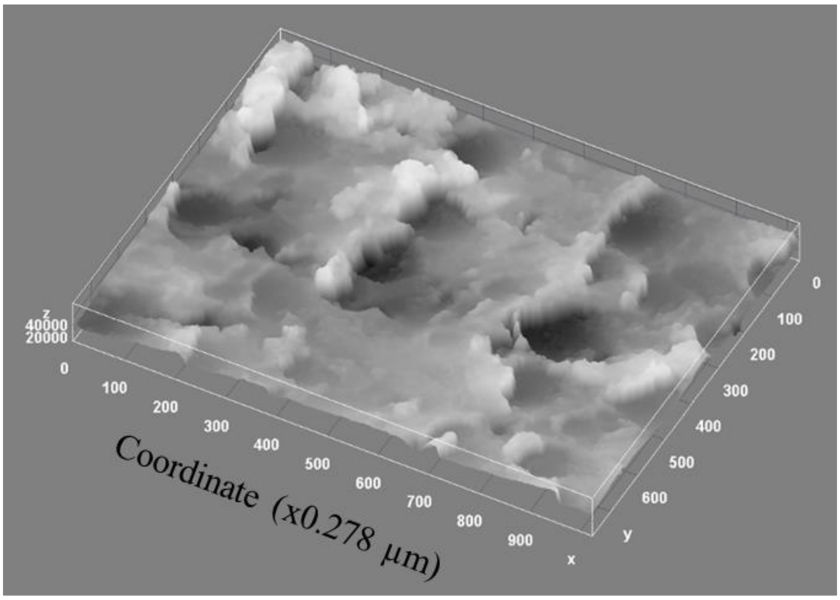


Figure 6.5: Asperities on polishing pad surface after 10 minutes polishing in the case of VRP, forward 360º backward 360º at point I

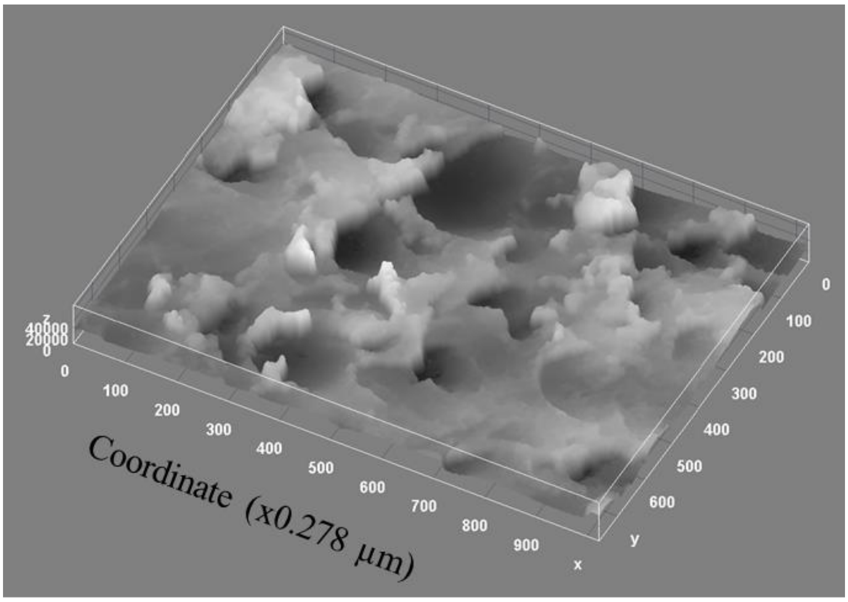


Figure 6.6: Asperities on polishing pad surface after 10 minutes polishing in the case of conventional polishing at point II

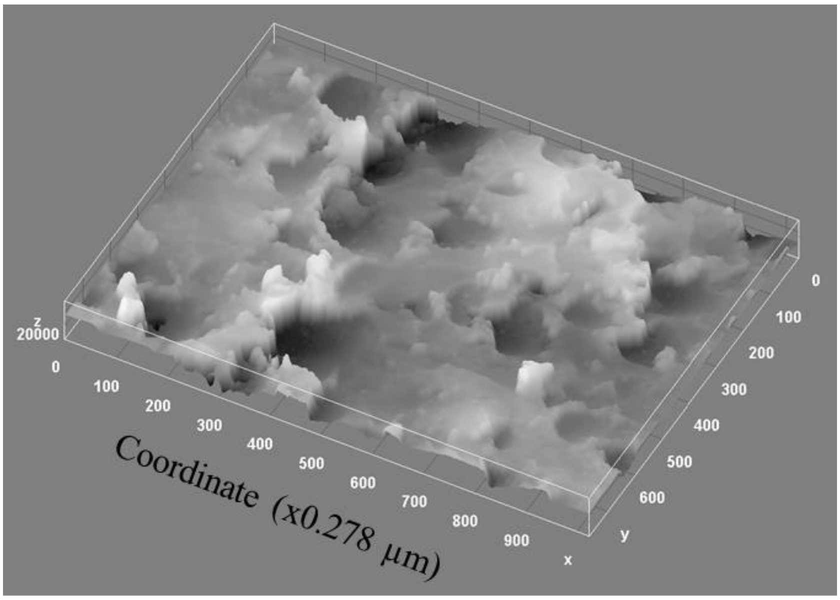
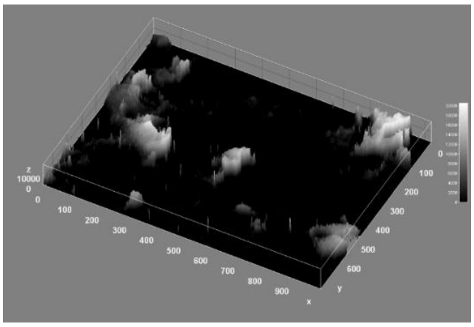
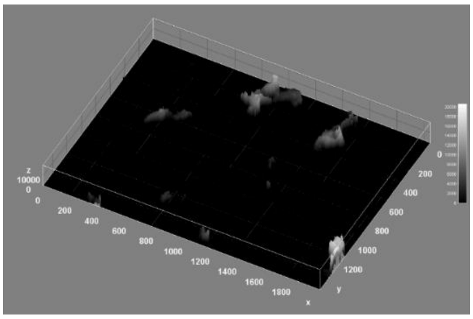


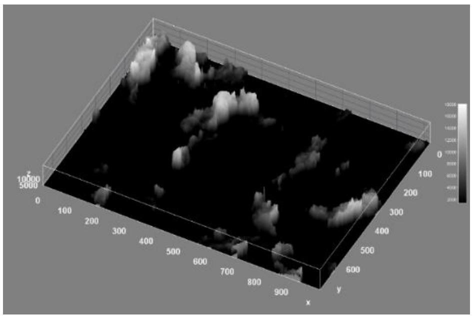
Figure 6.7: Asperities on polishing pad surface after 10 minutes polishing in the case of VRP, forward 360º backward 360º at point II



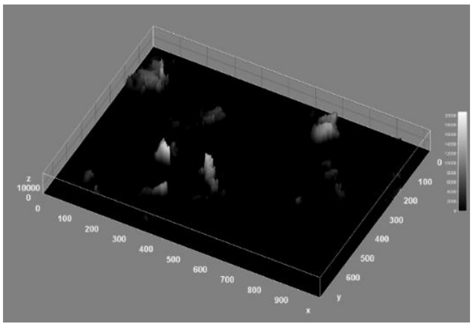
(a) After conditioning treatment



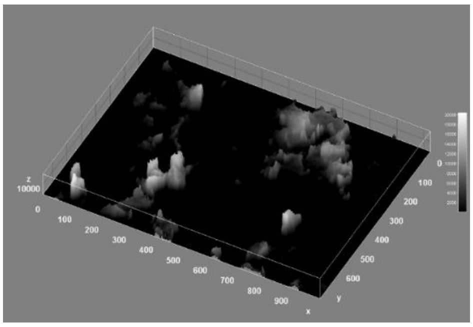
(b-1) Conventional polishing point I



(c-1) VRP, forward 360º backward 360º point I



(b-2) Conventional polishing point II



(c-2) VRP, forward 360º backward 360º point II

Figure 6.8: 20 μm of asperities height on the top of polishing pad surface: (a) after conditioning treatment, and after 10 minutes polishing (b) in the case of conventional polishing at point I, II (c) in the case of VRP, forward 360º backward 360º at point I, II

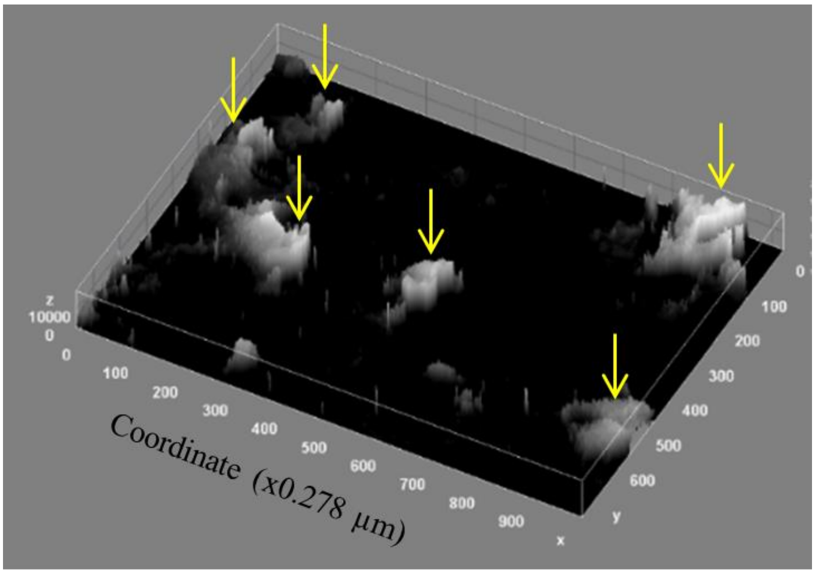


Figure 6.9: 20 µm of asperities height on the top of polishing pad surface after conditioning treatment

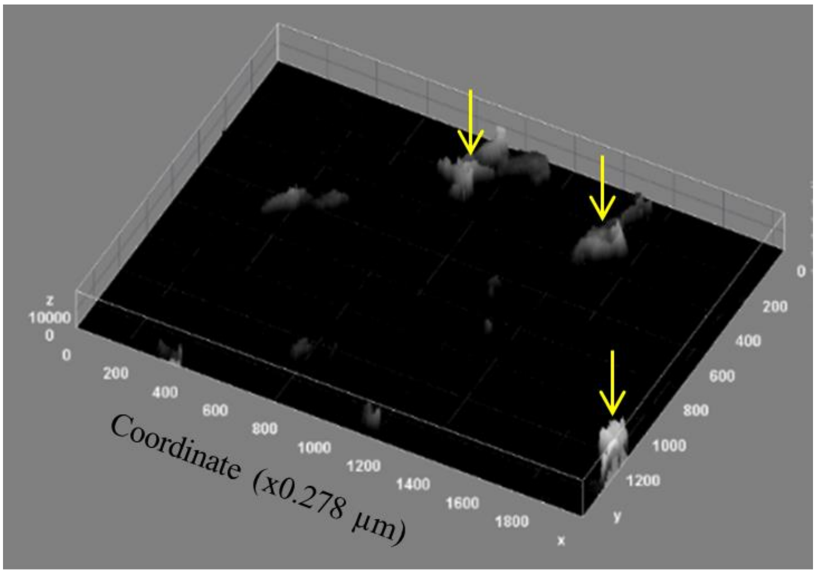


Figure 6.10: 20 μm of asperities height on the top of polishing pad surface after 10 minutes polishing in the case of conventional polishing at point I

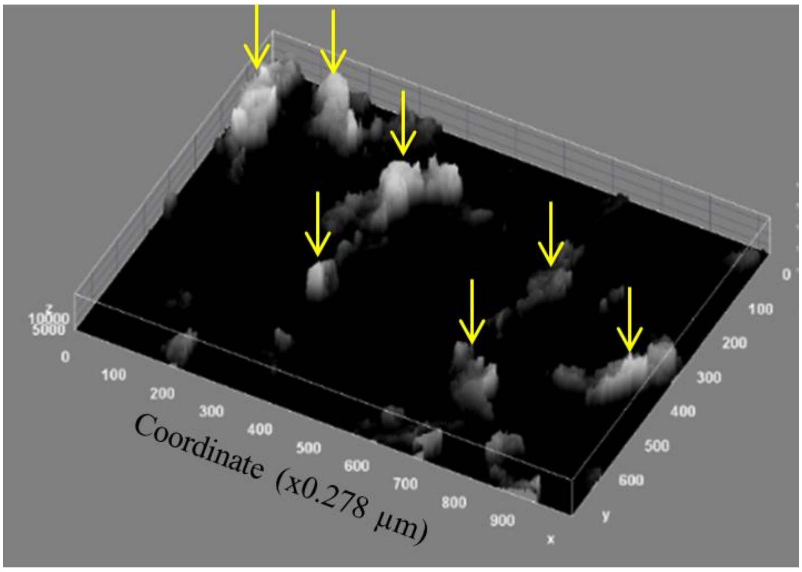


Figure 6.11: 20 μm of asperities height on the top of polishing pad surface after 10 minutes polishing in the case of VRP, forward 360º backward 360º at point I

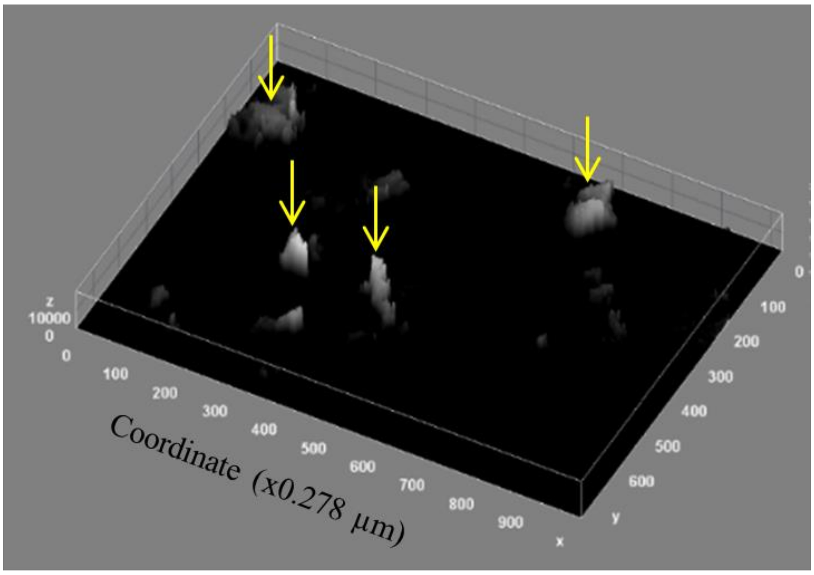


Figure 6.12: 20 µm of asperities height on the top of polishing pad surface after 10 minutes polishing in the case of conventional polishing at point II

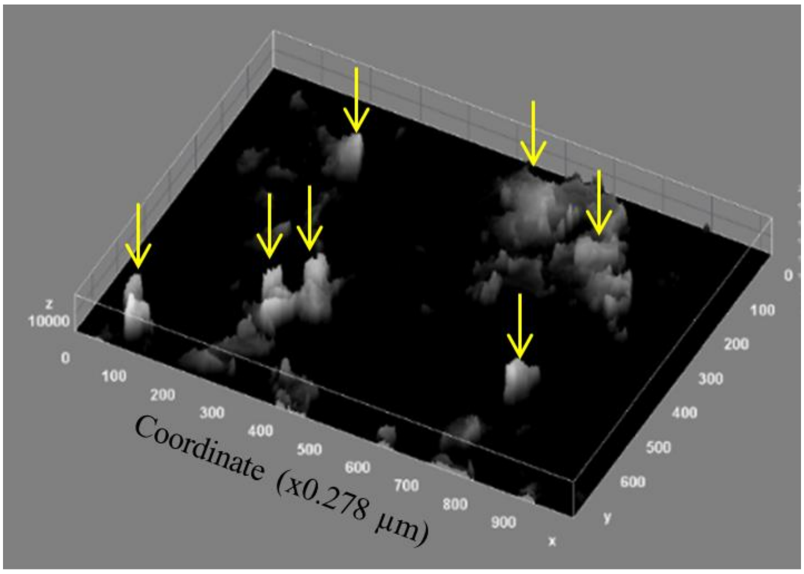


Figure 6.13: 20 µm of asperities height on the top of polishing pad surface after 10 minutes polishing in the case of VRP, forward 360º backward 360º at point II

6.2.2 Histogram of asperity height on polishing pad surface

In this topic, the histogram is used for an additional analysis from the 3 criteria. In the topic of 6.2.1, the top of 20 µm of asperities height on the top of polishing pad surface is used to find the relationship and difference among the 3 criteria by using image processing and analysis with ImageJ version 1.48 for analysis.

The histogram of 20 µm of asperities height on the top of polishing pad surface is shown in Figures 6.14 and 6.15. Figures 6.16 - 6.20 show the histogram of 20 µm of asperities height on the top of polishing pad surface in the case of conventional polishing where the height of gap disappears around the ellipse area and the histogram is different from the one with Variable Rotation Polishing method. Also, the histograms of 20 µm of asperities height on the top of polishing pad surface between conventional polishing and after conditioning treatment are different. However, in case of VRP method and after conditioning treatment, the histograms were similar especially the ellipse area where the height of histogram remains the same and they have similar appearance.

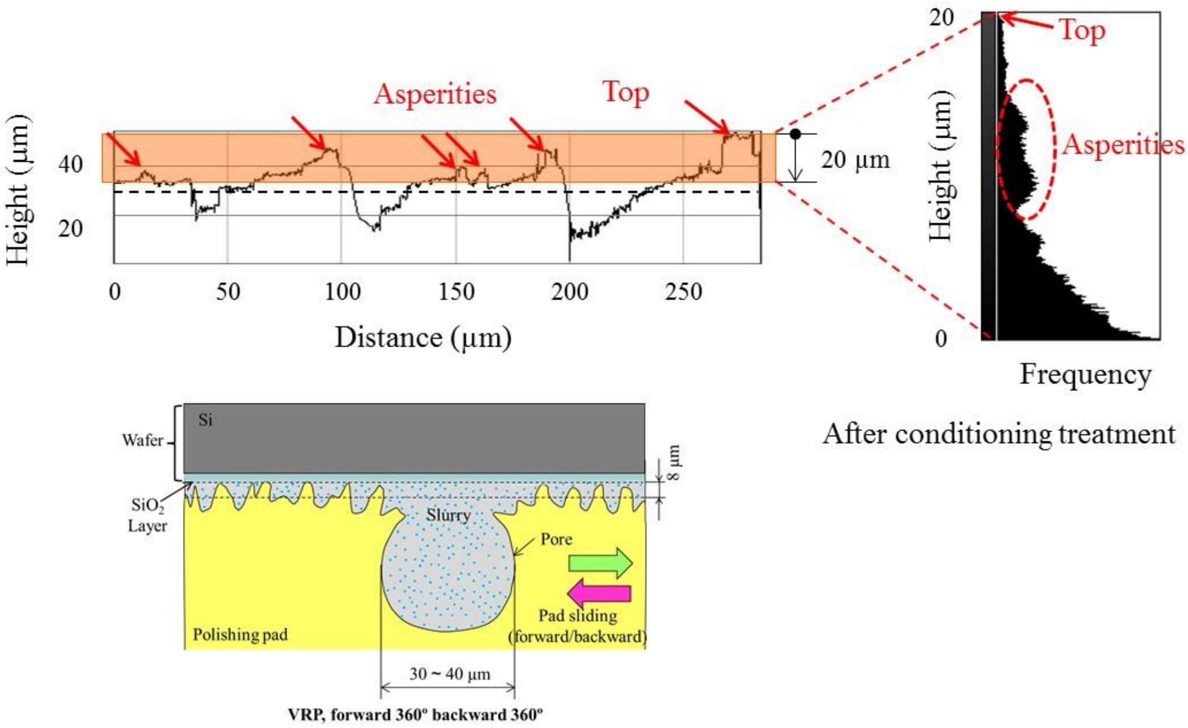


Figure 6.14: Difference of histogram of 20 μm of asperities height on the top of polishing pad surface

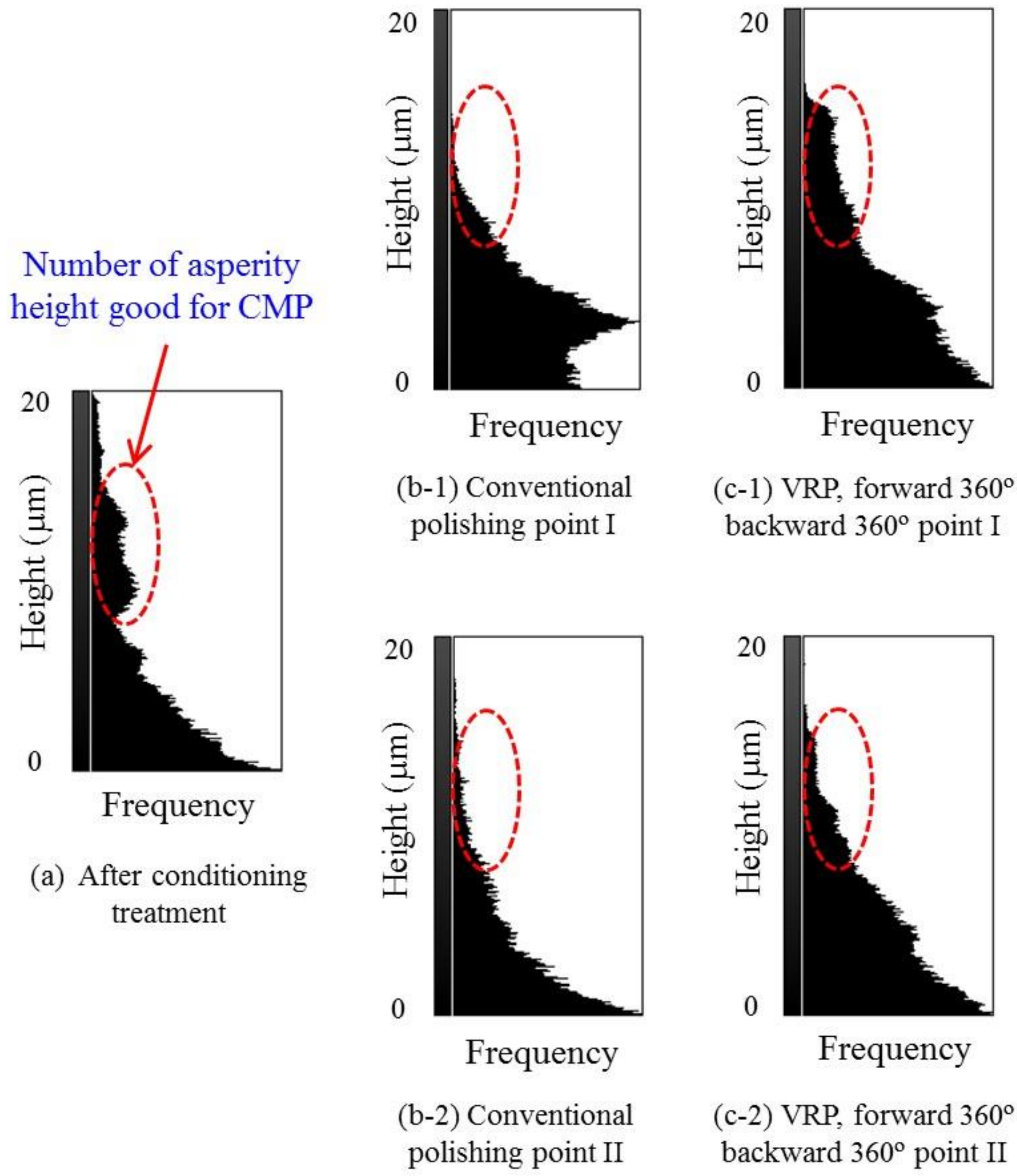


Figure 6.15: Difference of histogram of 20 μm of asperities height on the top of polishing pad surface: (a) after conditioning treatment, and after 10 minutes polishing (b) in case of conventional polishing point I,II (c) in case of VRP, forward 360º backward 360º point I,II

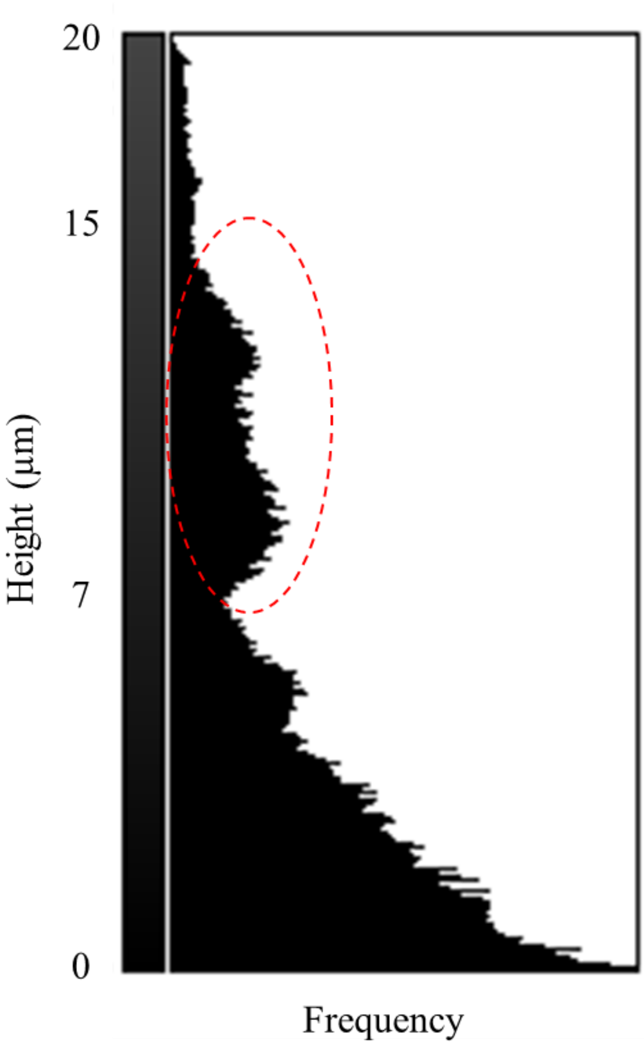


Figure 6.16: Difference of histogram of 20 µm of asperities height on the top of polishing pad surface after conditioning treatment

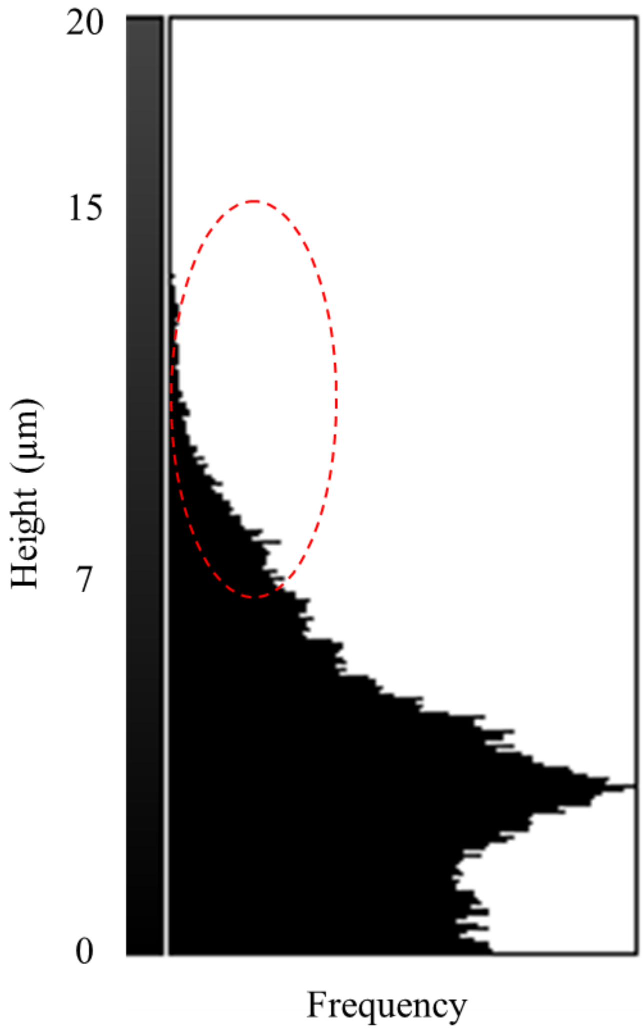


Figure 6.17: Difference of histogram of 20 µm of asperities height on the top of polishing pad surface after 10 minutes polishing in case of conventional polishing point I

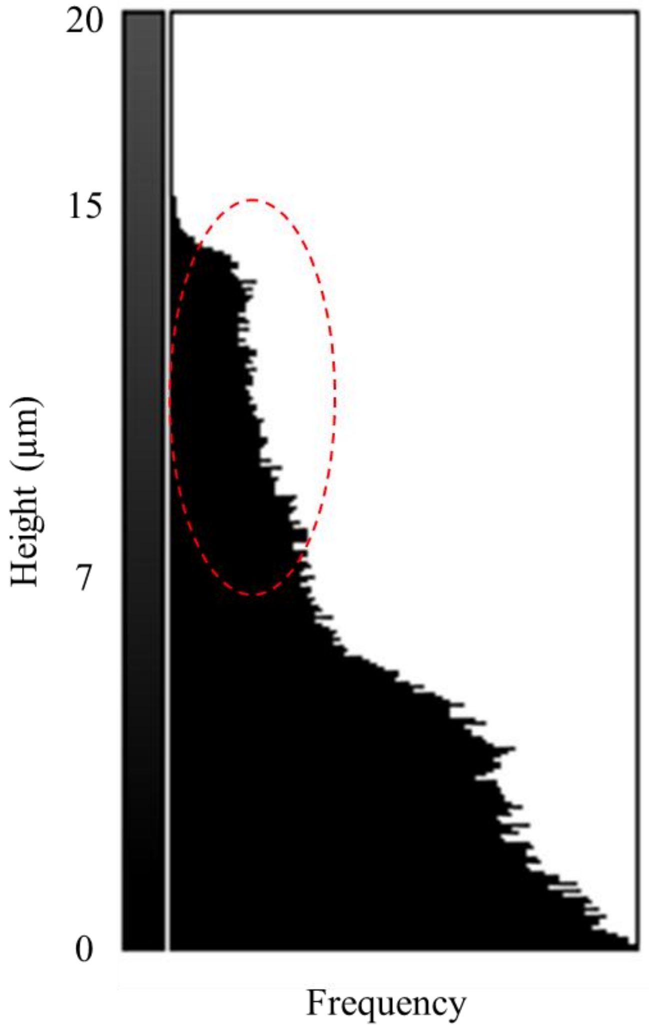


Figure 6.18: Difference of histogram of 20 μm of asperities height on the top of polishing pad after polishing time of 10 in case of VRP, forward 360º backward 360º point I

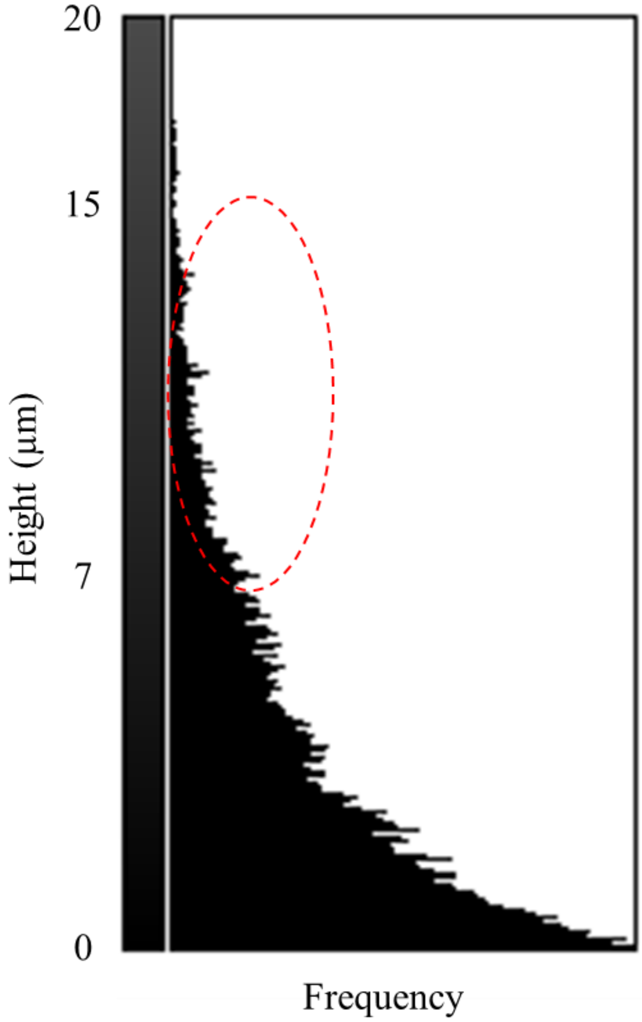


Figure 6.19: Difference of histogram of 20 µm of asperities height on the top of polishing pad surface after 10 minutes polishing in case of conventional polishing point II

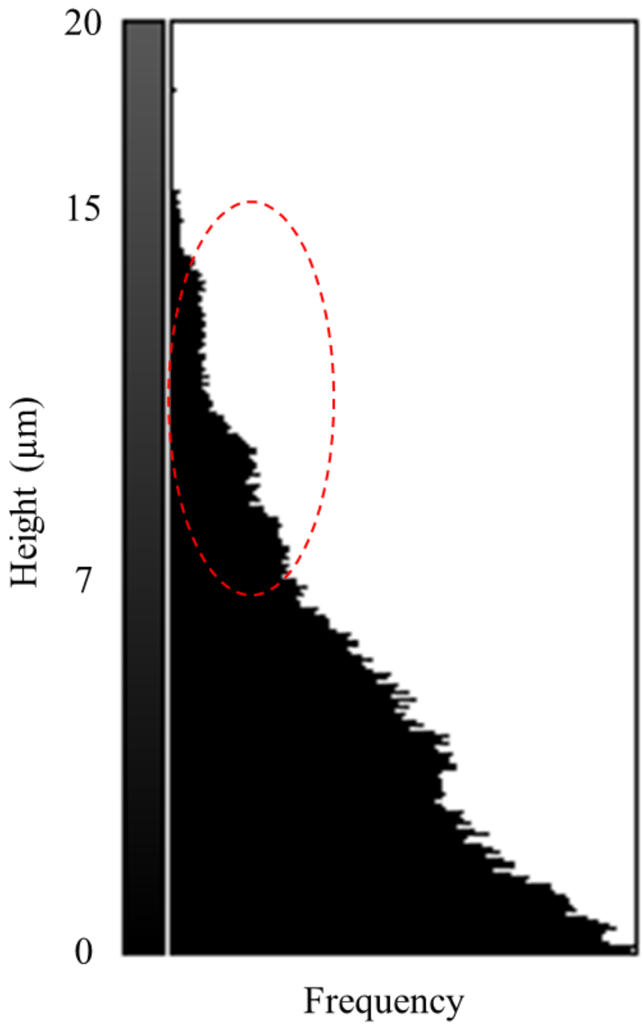


Figure 6.20: Difference of histogram of 20 μm of asperities height on the top of polishing pad after polishing time of 10 in case of VRP, forward 360º backward 360º point II

6.3 Discussion

6.3.1 3D topography observation

As a result from Figures 6.8 – 6.13, there were less asperities at the height below 20 μm from the top of polishing pad surface in case of conventional polishing because the asperities were bent to one direction at all polishing time resulting in the lower asperities height. With this reason, the material removal rate decreased along the polishing time.

On the other hand, the asperity height with VRP method and after conditioning treatment were almost the same and still had many asperities at 20 μm from the top because the asperities were not bent to one direction at all polishing time and sustain asperities height (contact area). This means that during VRP method the asperity on polishing pad surface was maintained to stand and sustain material removal rate.

6.3.2 Histogram

The ellipse on each histogram shows the top of asperities at the height of 7 – 15 μm expecting to be a part of contact areas between the top of asperities and the wafer surface which is the key point affecting the polishing. Figures 6.16 - 6.20 show that the histograms of 20 μm of asperities height on the top of polishing pad surface between conventional polishing and after conditioning treatment are different. Because of conventional polishing in the ellipse, the height of the histogram disappears. This means that the asperities at the height around 7 – 15 μm disappear after 10 minutes polishing. With this reason, MRR is decreased when the polishing time is increased. The conventional polishing then needs conditioning treatment in order to restore the asperities at the height of around 7 – 15 μm.

On the other hand, in case of VRP method and after conditioning treatment were similar histogram especially in the ellipse area where the height of the surface remains. This shows that the asperities at the height of around 7 – 15 μm remain after 10 minutes polishing. In summary, the VRP method can maintain the asperities at this height level same as the asperities after conditioning treatment. With this reason, MRR was not decreased even though the increase of polishing time.

6.4 Summary

According to investigation of 20 μm of asperities height on the top of polishing pad surface, the results from conventional polishing and Variable Rotation Polishing method were evidently different. The asperity heights with VRP method and after conditioning treatment represent similar histogram but there were less asperity below 20 μm from the top from conventional polishing. Asperities height with conventional polishing was bent to one direction for all polishing time resulting in the lower asperities height. On the other hand, for Variable Rotation Polishing method, asperities height was bent to back and forth direction for all polishing time, and sustains asperities height. It means that the VRP method can keep the asperity on polishing pad surface to stand, then it can sustain material removal rate.

Chapter 7

Conclusions

The variable rotation polishing method is proposed and subsequently experimentally investigated in order to improve polishing performance for the next generation of wafer size. The conclusions are as follows:

I. In the case of Variable Rotation Polishing, asperities of the polishing pad were bent and maintained to stand upright as well as preserved by backward direction rotation during CMP process. This behavior indicated that the preservation of the asperity on polishing pad surface would sustain the material removal rate. For these reasons, the conditioning treatment would be less unnecessary for CMP process with VRP method and could achieve cost reduction and longer pad life. Therefore, the asperity of polishing pad surface is a dominant parameter.

II. Material removal rate of the Variable Rotation Polishing was higher than conventional polishing. In the case of 360 degree backward rotation of the VRP method, the material removal rate was 38 percent higher than conventional polishing.

III. The slurry flow distribution in the Variable Rotation Polishing method becomes poor because the asperity were preserved due to bending in back and forth directions. Furthermore, the thickness of the slurry film at the case of Variable Rotation Polishing was approximately 1 μm thinner than that of conventional polishing. This smaller gap between wafer and polishing pad would also perform larger shear force and consequently affect the MRR.

References

[1] Back-end service. (2014, April 1). Retrieved November 18, 2014, from http://www.samsung.com/global/business/semiconductor/foundry/service/back-end-service.

[2] Joseph M. Steigerwald, et al, " Chemical Mechanical Planarization of Microelectronic Materials," 1997, p. 17

[3] N. Ohashi,et al., Proceeding of IITC, 140, 2001.

[4] Introduction of the semiconductor fabrication processing. (2013, October 23). Retrieved November 26, 2014, from http://rohitrana33.blogspot.jp/2013/10/introduction-of-semiconductor.html

[5] S. Sugimoto, et al, " Recent Progress of Semiconducter Process Techinologies and Future Challenges, " Toshiba Review vol.59 No.8, 2004, pp. 2-7.

[6] Suresh Babu Yeruva, "Particle Scale Modelling of Material Removal and Surface Roughness in Chemical Mechanical Polishing," University of Florida's Dissertation, December 2005, pp.11-12.

[7] Chao-Chang A. Chen, Ming-Hui Fang, C.Z. Feng, I-Peng Yao, Yung-Chang Hung, Kun-Cheng Tsai, "Analysis on Polishing Properties of CMP Pads," in *Proc. International Conference on Planarization/CMP Technology*, November 2008, p. 65.

[8] Keiichi Kimura, Yuichi Hashiyama, Panart Khajornrungruang, Hirokuni Hiyama and Yoshihiro Mochizuki, "Study on material removal Phenomena in CMP process," in *Proc. International*

Conference on Planarization/CMP Technology, October 2007, Dresden, pp. 201-205.

[9] Keiichi Kimura, Keisuke Suzuki and Panart Khajornrungruang, "Study on fine particle behavior in slurry flow between wafer and polishing pad as a material removal process in CMP," in *Proc. International Conference on Planarization/CMP Technology*, October 2012, Grenoble, France, pp. 345-350.

[10] Leonard Borucki and Ara Philipossian, "An analysis of potential 450 mm CMP tool scaling questions," *Solid state technology*, December 2009, pp. 10-13.

[11]Keiichi Kimura, Panart Khajornrungruang, Yuichi Hashiyama and Keisuke Suzuki, "Study on material removal mechanism in CMP process for SiO_2 film 1st report -Material remove function of fine particles in slurry," in *Proc. JSPE*, 2010, pp. 147-148 (in Japanese).

[12] F.W. Preston , J Soc. Glass Technol., November 1927, p. 247.

[13] Panart Khajornrungruang, Keiichi Kimura, A. Baba, K. Yasuda, Akiho Tanaka. (2010). Development of Orderly Micro Asperity on Polishing Pad Surface for Chemical Mechanical Polishing (CMP) Process using Anisotropic Etching. *AIJSTPME,* pp.29-34.

[14]Cheolmin Shin, Hojoong Kim and Taesung Kim, "A Study on the Shape of Abrasive Pattern on CMP Conditioner and Their Effect on Coefficient of Friction," in *Proc. International Conference on Planarization/CMP Technology*, 2013, pp. 226-227.

[15] RK Singh, A Galpin, P Doering, DWells, K Chiu and C Vroman, "Development and Performance Characterization of Next-Generation

CMP Pad Conditioners," in *Proc. International Conference on Planarization/CMP Technology*, 2013, pp. 72-79.

[16] Koki OYAMA, Toshiro K.Doi, Hideo AIDA, Syuhei KUROKAWA, Yasuhisa SANO, Hidetoshi TAKEDA, Koji KOYAMA,Tsutomu YAMAZAKI and Kunimitsu TAKAHASHI, "Diamond substrate planarization polishing technique," in *Proc. International Conference on Planarization/CMP Technology*, 2013, pp. 307-309.

[17] T. Doi, "Detail of Semiconductor CMP Technology," Kogyo Chosakai Publiching Co., Ltd., 2001,

[18] Tsutomu Yamazaki, Toshiro K. Doi, Michio Uneda, Syuhei Kurokawa, Osamu Ohnishi, Kiyoshi Seshimo and Hideo Aida. (2012). Effect of Groove Pattern of Chemical Mechanical Polishing Pad on Slurry Flow Behavior. *Japanese Journal of Applied Physics 51*, pp. 05EF03-1 - 05EF03-2

[19] Michio Uneda, Tatsunori Omote, Kazutaka Shibuya, Yoshio Nakamura, Daizo Ichikawa and Ken-ichi Ishikawa, "Evaluation for In-Plain Micro-Deformation Distribution Characteristics of Polishing Pad Surface Texture," in *Proc. ADMETA plus 2012*, October 2012, pp. 94-95.

[20] Michio Uneda, Yuya Fukuta, Yasuaki Itou, Kazutoshi Hotta, Kazusei Tamai, Hitoshi Morinaga and Ken-ichi Ishikawa, "Relationships between Polishing Variables, Removal Rate and Slurry Flow in Sapphire-CMP," in *Proc. International Conference on planarization/CMP Technology*, 2013, pp. 277-280.

[21] Michio Uneda, Yoshihiro Takahashi, Kazutaka Shibuya, Yoshio Nakamura, Daizo Ichikawa and Ken-ichi Ishikawa, "Relationships Between Removal Rate, Pad Surface Asperity and Polishing Head Vibration in Si-CMP," in *Proc. International Conference on Planarization/CMP Technology*, 2013, pp. 214-217.

[22] Dipto G. Thakurta, Christopher L. Borst, Donald W. Schwendaman, Ronald J. Gutmann, William N. Gill. (2000). Pad porosity, compressibility and slurry delivery effects in chemical mechanical planarization: modeling and experiments. *Elsevier*, *Thin Solid Films 366*, pp. 181-190.

[23] Jingang Yi. (2005, Aug.). On the Wafer/Pad Friction of Chemical–Mechanical Planarization (CMP) Processes—Part I: Modeling and Analysis. *IEEE Transactions on Semiconductor Manufacturing*, 18 No.3 pp. 359-370.

[24] Akiho Tanaka, Keisuke Suzuki, Panart Khajornrungruang, Suguru Takahashi and Keiichi Kimura, "Study on the material removal mechanism of SiO_2-CMP," in *Proc. International Conference on Planarization/CMP Technology*, November 2011, pp. 341-346.

[25] C. Rogers, J. Coppeta, L. Racz,A. Philipossian, F.B. Kaufman and D.Bramono, *Analysis of Flow Between a Wafer and Pad During CMP Processes, Special Issue Paper Journal of Electronic Materials*, 27 No. 10, (1998), pp. 1082-1087.

[26] N. Yoshizawaa, H. Nakane, T. Negishi, Y. Shimada, T. Kikuchi, K. Arai. *(2002)*. Spatial resolution measurement of giant magneto-

resistance thin film. *Journal of Magnetism and Magnetic Materials,* 239, pp. 198–200.

[27] G. Bahar Basim, Ivan U. Vakarelski, and Brij M. Moudgil, “Role of interaction forces in controlling the stability and polishing performance of CMP slurries, Journal of Colloid and Interface Science,” 263 (2003), pp. 506–515.

[28] S.H. Li, R.O. Miller, “Chemical Mechanical Polishing in Silicon, Semiconductors and Semimetals,” vol. 63, Academic Press, 2000.

[29] Pipat Phaisalpanumas, Keisuke Suzuki, Keiichi Kimura and Panart Khajornrungruang, “Study on Variable Rotation Polishing Method in CMP Process - Investigation of forward and backward rotation parameters –,” in *Proc. International Conference onPlanarization /CMP Technology*, October-November 2013, pp. 220-223.

[30] Panart Khajornrungruang, Keiichi Kimura, Ryuji yui, Nagisa Wada and Keisuke Suzuki. *(2011).* Slurry Supplying Method for Large Quartz Glass Substrate Polishing. *Japanese Journal of Applied Physics 50,* pp. 05EC03-1-05EC03-2.

[31] LT-9010M Model’s specification. (2014, April 1). Retrieved November 18, 2014, from http://www.keyence.com/products/measure/laser-confocal/lt-9000/models/lt-9010m/index.jsp.

[32] Hironobu Fukagawa, Keisuke Suzuki, Panart Khajornrungruang and Keiichi Kimura, “Measurement of slurry film thickness during CMP,” in *Proc. International Conference on Planarization/CMP Technology*, November 2011, pp. 118-122.

[33] S. Lawing, "Pad conditioning effects in chemical mechanical polishing," in: China 2004 SEMI Technology Symposium, China, 2004.

[34] J. McGrath, C. Davis, "Polishing pad surface characterization in chemical mechanical planarization," J. Mater. Process. Technol. 153–154 (2004), pp. 666–673.

[35] K.H. Park, H.J. Kim, O.M. Chang, H.D. Jeong, "Effects of pad properties on material removal in chemical mechanical polishing," Journal of Materials Processing Technology, 187–188 (2007), pp. 73–76.

[36] J. Rittinger, S. Cvetkovic, L. Rissing, "Investigations on the removal mechanisms of diverse alumina based polishing slurries for chemical mechanical polishing of electro-plated NiFe 45/55," Microelectronic Engineering, 110 (2013), pp. 324–328.

[37] Hojoong Kim, Ha Sup Hwang and Taesung Kim, "Abrasive Material Type and Their Effect on Removal Rate Change Trend in Pad Lifetime," in *Proc. International Conference on Planarization/CMP Technology*, 2013, pp. 258-261.

[38] Dongwoo Kim, Yoonjung Gwon, Keejoon Oh, Hyunghwan Kim and Sungki Park, "Improvement of the Wafer Edge Uniformity at the Initial Pad Life Time in Poly-Si CMP by Using the Pre-Conditioned Pad," in *Proc. International Conference on Planarization/CMP Technology*, 2013, pp. 129-133.

[39] Keisuke Suzuki, Eiichiro Okamoto, Panart Khajornrungruang and Keiichi Kimura, "Study on contact image analysis between polishing pad and wafer during CMP," in *Proc. ADMETA* *plus* *2012*, October 2012, pp. 20-21.